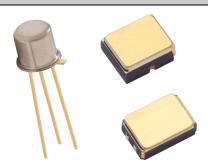


# **NPN Silicon, High-Speed Switching Transistors**

Rev. V1

#### **Features**

- JAN, JANTX, JANTXV, JANS and JANSR Qualified to MIL-PRF-19500/317
- · For Use in Military and High Reliability Applications
- TO-18 (TO-206AA), TO-46 (TO-206AB) and Surface Mount U, UA, and UB and Package Styles (See Mechanical Outlines for Specific Part/Package Availability)



# Electrical Characteristics (+25°C unless otherwise specified)

Parameter	Test Conditions		Units	Min.	Max.
Collector - Base Cutoff Current	V <sub>CB</sub> = 40 V dc	I <sub>CBO1</sub>	μA dc	_	10
Emitter - Base Cutoff Current	V <sub>EB</sub> = 4.5 V dc 2N2369A, 2N4449 V <sub>EB</sub> = 6.0 V dc 2N3227	I <sub>EBO1</sub>	μA dc	_	10
Breakdown Voltage Collector - Emitter	I <sub>C</sub> = 10 mA dc 2N2369A, 2N4449 2N3227		V dc	_	15 20
Collector - Emitter Cutoff Current	V <sub>CE</sub> = 20 Vdc	I <sub>CES</sub>	μA dc	_	0.4
Collector - Base Cutoff Current	V <sub>CB</sub> = 32 V dc	I <sub>CBO2</sub>	μA dc	_	0.2
Emitter - Base Cutoff Current	ent V <sub>EB</sub> = 4 V dc		μA dc	_	0.25
Forward Current Transfer Ratio	$V_{\text{CE}} = 0.35 \text{ V dc; } I_{\text{C}} = 10 \text{ mA dc}$ Forward Current Transfer Ratio $2N2369A, 2N4449$ $2N3227$		-	40 70	120 250
Forward Current Transfer Ratio	$V_{CE}$ = 0.4 V dc; $I_{C}$ = 30 mA dc 2N2369A, 2N4449 2N3227	h <sub>FE2</sub>	-	30 40	120 250
Forward Current Transfer Ratio	$V_{CE}$ = 1.0 V dc; $I_{C}$ = 10 mA dc 2N2369A, 2N4449 2N3227	h <sub>FE3</sub>	-	40 75	120 300
Forward Current Transfer Ratio	$V_{CE}$ = 1.0 V dc; $I_{C}$ = 100 mA dc 2N2369A, 2N4449 2N3227	h <sub>FE4</sub>	-	20 30	120 150



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# Electrical Characteristics (+25°C unless otherwise specified)

Parameter	Test Conditions		Units	Min.	Max.
Collector - Emitter Saturation Voltage	$I_C$ = 10 mA dc; $I_B$ = 1.0 mA dc	V <sub>CE(sat)1</sub>	V dc	_	0.20
Collector - Emitter Saturation Voltage	Emitter Saturation Voltage $I_C = 30 \text{ mA dc}$ ; $I_B = 3.0 \text{ mA dc}$		V dc	_	0.25
Collector - Emitter Saturation Voltage	$I_{C}$ = 100 mA dc; $I_{B}$ = 10 mA dc	V <sub>CE(sat)3</sub>	V dc	_	0.45
Base - Emitter Saturation Voltage	$I_C$ = 10 mA dc; $I_B$ = 1.0 mA dc	$V_{BE(sat)1}$	V dc	0.70	0.85
Base - Emitter Saturation Voltage	$I_C$ = 30 mA dc; $I_B$ = 3.0 mA dc	V <sub>BE(sat)2</sub>	V dc	_	0.90
Base - Emitter Saturation Voltage	$I_C$ = 100 mA dc; $I_B$ = 10 mA dc	V <sub>BE(sat)3</sub>	V dc	0.8	1.20
Collector - Base Cutoff Current	$T_A = +150^{\circ}C; V_{CB} = 20 \text{ V dc}$	I <sub>CBO2</sub>	μA dc	<u>—</u>	30
Collector - Emitter Cutoff Current	$T_A = +125^{\circ}C$ $V_{CE} = 10 \text{ V dc}; V_{BE} = 0.25 \text{ V dc}$	I <sub>CEX2</sub>	μA dc	_	30
Collector - Emitter Voltage Saturated	$T_A = +125^{\circ}C$ $I_C = 10 \text{ mA dc}; I_B = 1.0 \text{ mA dc}$	V <sub>CE(sat)4</sub>	V dc	_	0.3
Base - Emitter Saturated Voltage	$T_A = +125^{\circ}\text{C}$ $I_C = 10 \text{ mA dc}; I_B = 1.0 \text{ mA dc}$ 2N2369A, 2N4449 2N3227	V <sub>BE(sat)4</sub>	V dc	0.59 0.50	
Forward Current Transfer Ratio	$T_A = -55^{\circ}\text{C}$ $V_{CE} = 1.0 \text{ V dc}; I_C = 10 \text{ mA dc}$ $2N2369A, 2N4449$ $2N3227$	h <sub>FE5</sub>	-	20 40	
Base - Emitter Saturated Voltage	$T_A = -55^{\circ}C$ $I_C = 10 \text{ mA dc}; I_B = 1.0 \text{ mA dc}$	V <sub>BE(sat)5</sub>	V dc	_	1.02



# NPN Silicon, High-Speed Switching Transistors

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## Electrical Characteristics (+25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Magnitude of Small-Signal Short-Circuit Forward Current Transfer Ratio	$V_{CE}$ = 10 V dc; $I_{C}$ = 10 mA dc; f = 100 MHz	h <sub>FE</sub>		5.0	10
Open Circuit Output Capacitance	V <sub>CB</sub> = 5 V dc; I <sub>E</sub> = 0; 100 kHz <u>&lt;</u> f <u>&lt;</u> 1 Mhz	$C_{ m obo}$	pF	_	4.0
Input Capacitance (Output Open-Circuited)	V <sub>EB</sub> = 0.5 V dc; I <sub>C</sub> = 0; 100 kHz <u>&lt;</u> f≤1 Mhz 2N2369A, 2N4449 2N3227	C <sub>ibo</sub>	pF	_	5.0 4.0
Charge Storage Time	$I_C$ = 10 mA dc; $I_{B1}$ = 10 mA dc; $I_{B2}$ = 10 mA dc 2N2369A, 2N4449 2N3227	t <sub>s</sub>	ns	_	13 18
Turn-On Time	$I_C$ = 10 mA dc; $I_{B1}$ = 3.0 mA dc; $I_{B2}$ = -1.5 mA dc		ns	_	12
Turn-Off Time	$I_C$ = 10 mA dc; $I_{B1}$ = 3.0 mA dc; $I_{B2}$ = -1.5 mA dc 2N2369A, 2N4449 2N3227	t <sub>off</sub>	ns	_	18 25



# **NPN Silicon, High-Speed Switching Transistors**

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# Absolute Maximum Ratings (+25°C unless otherwise specified)

Ratings	Symbol	Value
Collector - Emitter Voltage  2N2369A, UA, UB 2N4449, UA, UB 2N3227, UA, UB 2N2369AU 2N4449U 2N3227U	V <sub>CEO</sub>	15 V dc 15 V dc 20 V dc 15 V dc 15 V dc 20 V dc
Collector - Base Voltage (All types)	V <sub>CBO</sub>	40 Vdc
Emitter - Base Voltage  2N2369A, UA, UB 2N4449, UA, UB 2N3227, UA, UB 2N2369AU 2N4449U 2N3227U	V <sub>EBO</sub>	4.5 V dc 4.5 V dc 6.0 V dc 4.5 V dc 4.5 V dc 6.0 V dc
Collector - Emitter Voltage (All types)	V <sub>CES</sub>	40 Vdc
Operating & Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-65°C to +200°C



# **NPN Silicon, High-Speed Switching Transistors**

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#### **Thermal Characteristics**

Types	Symbol	Max. Value
Thermal Resistance, Junction to Case  2N2369A 2N4449 2N3227	R <sub>eJC</sub>	150°C/W 150°C/W 150°C/W
Thermal Resistance, Junction to Solder Pad  2N2369AUA, UB 2N4449UA, UB 2N3227UA, UB  2N2369AU 2N4449U 2N3227U	$R_{ hetaJSP}$	210°C/W 210°C/W 210°C/W 290°C/W ( <sup>7)</sup> 290°C/W ( <sup>7)</sup> 290°C/W ( <sup>7)</sup>
Thermal Resistance, Junction to Ambient  2N2369A 2N4449 2N3227  2N2369AUA, UB 2N4449UA, UB 2N2369AU 2N4449U 2N3227U	R <sub>eJA</sub>	400°C/W 400°C/W 486°C/W 486°C/W 486°C/W 350°C/W (6) 350°C/W (6) 350°C/W (6)



# **NPN Silicon, High-Speed Switching Transistors**

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Types	Symbol	Max. Value
Power Dissipation T <sub>A</sub> = +25°C		
2N2369AUA, UB 2N4449UA, UB 2N3227UA, UB	P <sub>T</sub>	0.36 W <sup>(2)</sup> 0.36 W <sup>(2)</sup> 0.36 W <sup>(2)</sup>
2N2369AU 2N4449U 2N3227U		0.5 W <sup>(5)</sup> 0.5 W <sup>(5)</sup> 0.5 W <sup>(5)</sup>
Power Dissipation T <sub>C</sub> = +125°C		
2N2369AUA, UB 2N4449UA, UB 2N3227UA, UB	P <sub>T</sub>	0.36 W <sup>(3) (4)</sup> 0.36 W <sup>(3) (4)</sup> 0.36 W <sup>(3) (4)</sup>
Power Dissipation T <sub>SP</sub> = +125°C <sup>(1)</sup>		
2N2369AUA, UB 2N4449UA, UB 2N3227UA, UB	P <sub>T</sub>	0.36 W <sup>(3)</sup> 0.36 W <sup>(3)</sup> 0.36 W <sup>(3)</sup>

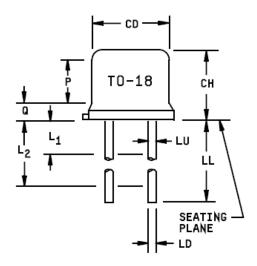
- (1) Applicable for UA, UB, and U packages.
- (2) For TO-18 and TO-46 packages derate linearly 2.06 mW/ $^{\circ}$ C above T<sub>A</sub> = +25 $^{\circ}$ C.
- (3) Derate linearly 4.8 mW/ $^{\circ}$ C above T<sub>C</sub> = +125 $^{\circ}$ C. See figures 8, 9, 10, 11 and 12 of MIL-PRF-19500/317
- (4) Power dissipation limited to 360 mW per chip regardless of thermal resistance.
- (5) For UA and UB, packages mounted on FR-4 PCB (1 Oz. Cu) with contacts 20 mils larger than package pads. See figure 13 of MIL=PRF-19500/317.
- (6) One side only, derate linearly 2.857 mW/ $^{\circ}$ C above  $T_{SP} = +25^{\circ}$ C.
- (7) Derate linearly 3.44 mW/°C above  $T_A = +54.5$ °C. See figure 13 of MIL-PRF-19500/317.

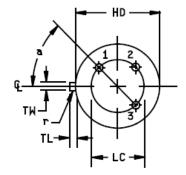


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## **Outline Drawing (TO-18)**

	Dimensions					
Ltr.	Inc	hes		neters	Notes	
	Min	Max	Min	Max		
CD	.178	.195	4.52	4.95		
CH	.170	.210	4.32	5.33		
HD	.209	.230	5.31	5.84		
LC	.100 TP		TP 2.54 TP		6	
LD	.016	.021	0.41	0.53	7,8	
LL	.500	.750	12.70	19.05	7,8,13	
LU	.016	.019	0.41	0.48	7,8	
L <sub>1</sub>		.050		1.27	7,8	
L <sub>2</sub>	.250		6.35		7,8	
Р	.100		2.54		5	
Q		.030		0.76	5	
TL	.028	.048	0.71	1.22	3,4	
TW	.036	.046	0.91	1.17	3	
r		.010		0.25	10	
α	45°	TP	45°	TP	6	





- 1. Dimension are in inches.
- 2. Millimeters are given for general information only.
- 3. Beyond r (radius) maximum, TH shall be held for a minimum length of .011 (0.28 mm).
- 4. Dimension TL measured from maximum HD.
- 5. Body contour optional within zone defined by HD, CD, and Q.
- Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
- Dimension LU applies between L<sub>1</sub> and L<sub>2</sub>. Dimension LD applies between L<sub>2</sub> and LL minimum. Diameter is uncontrolled in L<sub>1</sub> and beyond LL minimum.
- 8. All three leads.
- 9. The collector shall be internally connected to the case.
- 10. Dimension r (radius) applies to both inside corners of tab.
- 11. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi x$  symbology.
- 12. Lead 1 = emitter, lead 2 = base, lead 3 = collector.

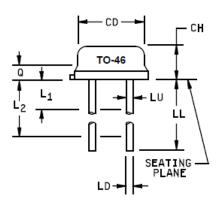
FIGURE 1. Physical dimensions TO-18 (2N2369A and 2N3227).

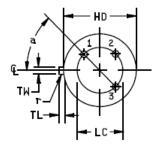


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## **Outline Drawing (TO-46)**

		Dimo	nciono		
	<b>—</b> .		nsions		
Ltr.		ches	-	neters	Notes
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.065	.085	1.65	2.16	
HD	.209	.230	5.31	5.84	
LC	.10	.100 TP 2.54 T		4 TP	5
LD	.016	.021	0.41	0.53	
LL	.500	1.750	12.70	44.45	6
LU	.016	.019	0.41	0.48	6
L <sub>1</sub>		.050		1.27	6
L <sub>2</sub>	.250		6.35		6
Q		.040		1.02	3
TL	.028	.048	0.71	1.22	8
TW	.036	.046	0.91	1.17	4
r		.010		0.25	9
α	45	45° TP		° TP	5





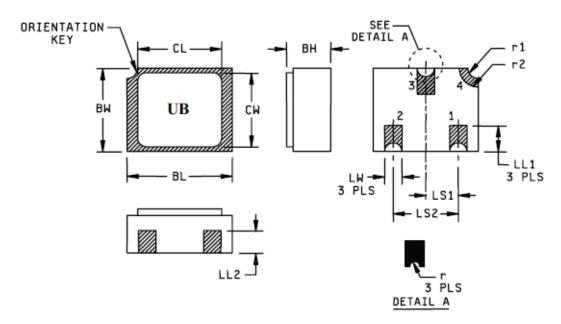
- Dimensions are in inches.
- 2. Millimeters are given for general information only.
- Symbol TL is measured from HD maximum.
- 4. Details of outline in this zone are optional.
- Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of TP relative to tab. Device may be measured by direct methods or by gauge.
- 6. Symbol LU applies between L<sub>1</sub> and L<sub>2</sub>. Dimension LD applies between L<sub>2</sub> and LL minimum.
- 7. Lead number three is electrically connected to case.
- 8. Beyond r maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
- Symbol r applied to both inside corners of tab.
- 10. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.
- 11. Lead 1 is emitter, lead 2 is base, and lead 3 is collector.

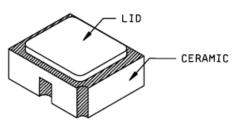
FIGURE 2. Physical dimensions - TO-46 (2N4449).

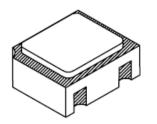


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#### **Outline Drawing (UB)**







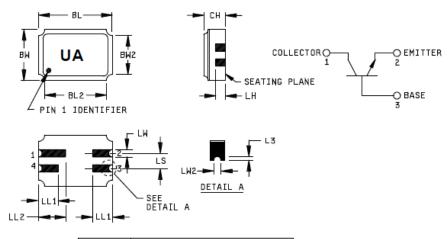
	Dimensions						
Symbol	Inc	hes	Millim	neters			
	Min.	Max.	Min.	Max.			
ВН	0.046	0.056	1.17	1.42			
BL	0.115	0.128	2.92	3.25			
BW	0.085	0.108	2.16	2.74			
CL	_	0.128		3.25			
CW		0.108		2.74			
LL1	0.022	0.038	0.56	0.96			
LL2	0.017	0.035	0.43	0.89			
LS1	0.036	0.040	0.91	1.02			
LS2	0.071	0.079	1.81	2.01			
LW	0.016	0.024	0.41	0.61			
r	_	0.008	_	0.203			
r1	_	0.012	_	0.305			
r2	_	0.022	_	0.559			

Figure 3. Physical dimensions, surface mount (UB) for 2N2369A, 2N3227 and 2N2449



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#### **Outline Drawing (UA Surface Mount)**



	Dimensions				
Ltr.	Inches		Milli	meters	
	Min	Max	Min	Max	
BL	.215	.225	5.46	5.71	
BL2		.225		5.71	
BW	.145	.155	3.68	3.93	
BW <sub>2</sub>		.155		3.93	
CH	.061	.075	1.55	1.90	
L3	.003		0.08		
LH	.029	.042	0.74	1.07	
LL <sub>1</sub>	.032	.048	0.81	1.22	
LL <sub>2</sub>	.072	.088	1.83	2.23	
LS	.045	.055	1.14	1.39	
LW	.022	.028	0.56	0.71	
LW2	.006	.022	0.15	0.56	

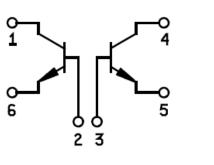
Pin number.	1	2	3	4
Transistor	Collector	Emitter	Base	N/C

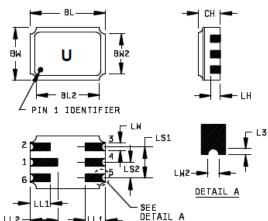
- Dimensions are in inches.
- Millimeters are given for general information only.
- Dimension CH controls the overall package thickness. When a window lid is used, dimension CH must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
- The corner shape (square, notch, radius) may vary at the manufacturer's option, from that shown on the drawing.
- 5. Dimensions LW2 minimum and L3 minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on the bottom two layers, optional on the top ceramic layer.) Dimension LW2 maximum define the maximum width of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
- The co-planarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15mm) for solder dipped leadless chip carriers.
- In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.
- \* FIGURE 4. Physical dimensions surface mount (UA version, 2N2369AUA, 2N3227UA, and 2N4449UA)



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#### **Outline Drawing (U)**





		Din	nensions	
Ltr.	Inc	hes	Millim	eters
	Min	Max	Min	Max
BL	.240	.250	6.10	6.35
BL <sub>2</sub>		.250		6.35
BW	.165	.175	4.19	4.44
BW <sub>2</sub>		.175		4.44
CH	.066	.080	1.68	2.03
L <sub>3</sub>	.003	.007	0.08	0.18
LH	.026	.039	0.66	0.99
LL <sub>1</sub>	.060	.070	1.52	1.78
LL <sub>2</sub>	.082	.098	2.08	2.49
LS <sub>1</sub>	.095	.105	2.41	2.67
LS <sub>2</sub>	.045	.055	1.14	1.39
LW	.022	.028	0.56	0.71
LW <sub>2</sub>	006	022	0.15	0.56

Pin number	1	2	3	4	5	6
Transistor	Collector no. 1	Base no. 1	Base no. 2	Collector no. 2	Emitter no. 2	Emitter no. 1

- Dimensions are in inches.
- Millimeters are given for general information only.
- Dimension CH controls the overall package thickness. When a window lid is used, dimension CH must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
- The corner shape (square, notch, radius) may vary at the manufacturer's option, from that shown on the drawing.
- 5. Dimensions LW2 minimum and L3 minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on the bottom two layers, optional on the top ceramic layer.) Dimension LW2 maximum and L3 maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
- The co-planarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15mm) for solder dipped leadless chip carriers.
- In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.
  - \* FIGURE 5. Physical dimensions surface mount (dual transistors, U version only, 2N2369AU, 2N3227U, and 2N4449U).



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#### **Thermal Impedance Curves**

#### Maximum Thermal Impedance

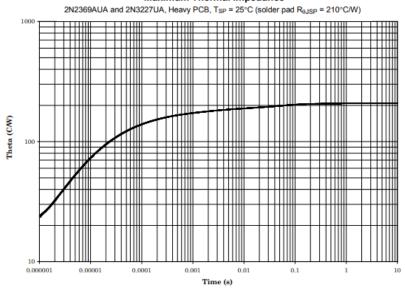


FIGURE 8. Thermal impedance graph (R<sub>0JSP</sub>) for 2N2369AUA and 2N3227UA.

#### **Maximum Thermal Impedance**

2N2369AUB, 2N2369AUBC, 2N3227UB, and 2N3227UBC Heavy PCB, T<sub>SP</sub> = 25°C (solder pad R<sub>0JSP</sub> = 210°C/W)

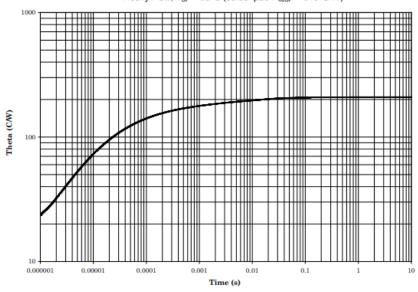


FIGURE 9. Thermal impedance graph (R<sub>9JSP</sub>) for 2N2369AUB, 2N2369AUBC, 2N3227UB, and 2N3227UBC.



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#### **Thermal Impedance Curves**

# 

#### FIGURE 10. Thermal impedance graph TO-46 (R<sub>0,JA</sub>) for 2N4449.

Time (s)

# 

FIGURE 11. Thermal impedance graph (TO-18) (R<sub>0,JA</sub>) for 2N2369A and 2N3227.



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#### **Thermal Impedance Curves**

#### Maximum Thermal Impedance

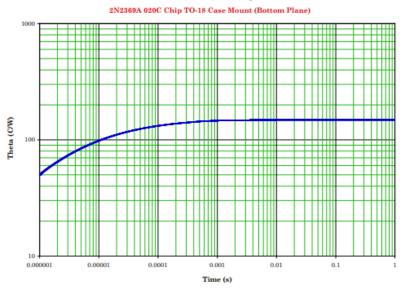


FIGURE 12. Thermal impedance graph (TO-18 TO-46) (RBJC) for 2N2369A.

#### **Maximum Thermal Impedance**

20x20 Chip in U LCC6 Pkg, Heavy PCB, Tsp=25C, @jsp=210C/W, Side 1 of 2

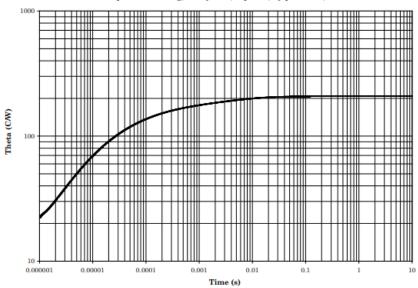


FIGURE 13. Thermal impedance graph (R<sub>BUSP</sub>) for 2N2369AU and 2N3227U.



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