

2N2484, 2N2484UA, 2N2484UB

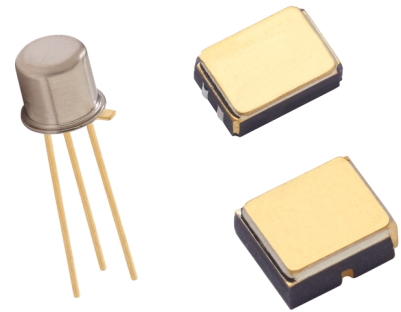


NPN Low Power Silicon Transistor

Rev. V3

Features

- Available in JAN, JANTX, JANTXV and JANS per MIL-PRF-19500/376
- Lightweight & Low Power
- Military & Other High Reliability Applications
- TO-18 (TO-206AA), TO-46 (TO-206AB) Surface Mount UA and UB Package Styles



Electrical Characteristics ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Collector - Emitter Breakdown Voltage	$I_C = 10 \text{ mA}$	$V_{(BR)CEO}$	V dc	60	—
Collector - Emitter Cutoff Current	$V_{CE} = 45 \text{ V dc}$	I_{CES}	nA dc	—	5
Collector - Base Cutoff Current	$V_{CB} = 60 \text{ V dc}$ $V_{CB} = 45 \text{ V dc}$	I_{CBO1}	$\mu\text{A dc}$	—	10
		I_{CBO2}	nA dc	—	5
Emitter - Base Cutoff Current	$V_{EB} = 6 \text{ V dc}$ $V_{EB} = 5 \text{ V dc}$	I_{EBO1}	$\mu\text{A dc}$	—	10
		I_{EBO2}	nA dc	—	2
Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V dc}; I_C = 1 \mu\text{A dc}$	h_{FE}	-	45	—
	$V_{CE} = 5 \text{ V dc}; I_C = 10 \mu\text{A dc}$			200	500
	$V_{CE} = 5 \text{ V dc}; I_C = 100 \mu\text{A dc}$			225	675
	$V_{CE} = 5 \text{ V dc}; I_C = 500 \mu\text{A dc}$			250	800
	$V_{CE} = 5 \text{ V dc}; I_C = 1 \text{ mA dc}$			250	800
	$V_{CE} = 5 \text{ V dc}; I_C = 10 \text{ mA dc}$			225	800
Collector - Emitter Saturation Voltage	$I_C = 1.0 \text{ mA dc}, I_B = 100 \mu\text{A dc}$	$V_{CE(SAT)}$	Vdc	—	0.3
Base - Emitter Saturation Voltage	$V_{CE} = 5 \text{ V dc}; I_C = 100 \mu\text{A dc}$	$V_{BE(on)}$	Vdc	0.5	0.7
Magnitude of Common Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio	$I_C = 50 \mu\text{A dc}; V_{CE} = 5 \text{ V dc}; 5 \text{ MHz}$ $I_C = 500 \mu\text{A dc}; V_{CE} = 5 \text{ V dc}; 30 \text{ MHz}$	$ h_{fe} _1$ $ h_{fe} _2$	-	3.0	7.0
				2.0	—
Collector - Base Cutoff Current	$T_A = +150^\circ\text{C}$ $V_{CB} = 45 \text{ V dc}$	I_{CBO3}	$\mu\text{A dc}$	—	10
Forward - Current Transfer Ratio	$V_{CE} = 5 \text{ V dc}; I_C = 10 \mu\text{A dc}$	h_{FE7}	-	35	—

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Parameter	Test Conditions	Symbol	Units	Min.	Max.
Small-Signal Open-Circuit Output Admittance	$I_C = 1.0 \text{ mA dc}; V_{CE} = 5 \text{ V dc}; f = 1 \text{ kHz}$	h_{OE}	μmhos	—	40
Small-Signal Open Circuit Reverse Voltage Transfer Ratio	$I_C = 1.0 \text{ mA dc}; V_{CE} = 5 \text{ V dc}; f = 1 \text{ kHz}$	h_{RE}	-	—	8×10^{-4}
Small-Signal Short-Circuit Input Impedance	$I_C = 1 \text{ mA dc}; V_{CE} = 5 \text{ V dc}; f = 1 \text{ kHz}$	h_{IE}	$k\Omega$	3.5	24.0
Small-Signal Short-Circuit Forward Current Transfer Ratio	$I_C = 1 \text{ mA dc}; V_{CE} = 5 \text{ V dc}; f = 1 \text{ kHz}$	h_{fe}	-	250	900
Open Circuit Output Capacitance	$V_{CB} = 5 \text{ V dc}; I_E = 0; 100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	C_{obo}	pF	—	5
Input Capacitance (Output Open-Circuited)	$V_{EB} = 5 \text{ V dc}; I_C = 0; 100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	C_{ibo}	pF	—	6.0

Absolute Maximum Ratings ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Ratings	Symbol	Value
Collector - Emitter Voltage	V_{CEO}	60 V dc
Collector - Base Voltage	V_{CBO}	60 V dc
Emitter - Base Voltage	V_{EBO}	6 V dc
Collector Current	I_C	50 mA dc
Total Power Dissipation ⁽¹⁾ @ $T_A = +25^\circ\text{C}$	P_T	360 mW
Operating & Storage Temperature Range	T_J, T_{STG}	-65°C to $+200^\circ\text{C}$

Thermal Characteristics

Characteristics	Symbol	Max. Value
Thermal Resistance, Junction to Ambient ⁽²⁾ 2N2484 2N2484UA 2N2484UB, UBC	$R_{\theta JA}$	325°C/W 275°C/W 350°C/W
Thermal Resistance, Junction to Solder Pad ⁽²⁾ 2N2484UA 2N2484UB, UBC	$R_{\theta JSP}$	110°C/W 100°C/W

(1) For derating see figure 7, figure 8 and figure 9 of MIL-PRF-19500/376

(2) For thermal impedance see figure 10, 11, 12, 13 and 14 of MIL-PRF-19500/376.

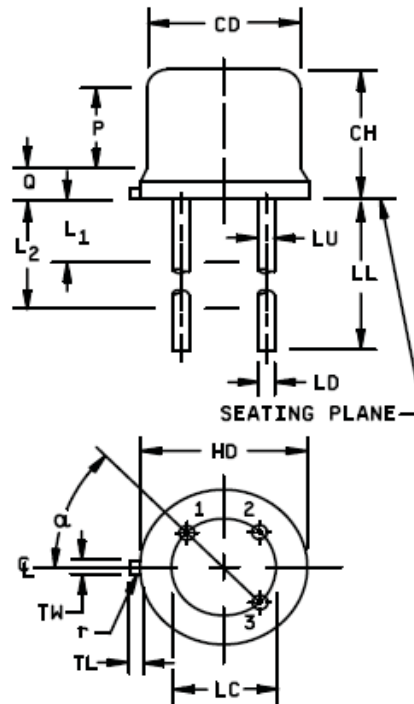
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Outline Drawing (TO-18)



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TL shall be held for a minimum length of .011 inch (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane $.054 +.001 -.000$ inch ($1.37 +0.03 -0.00$ mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L_1 and L_2 . Dimension LD applies between L_2 and LL minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
12. Lead 1 = emitter, lead 2 = base, lead 3 = collector.
13. For L suffix devices, dimension LL = 1.5 inches (38.10 mm) min. and 1.75 inches (44.45 mm) max.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.70	19.05	7,8,13
LU	.016	.019	0.41	0.48	7,8
L_1		.050		1.27	7,8
L_2	.250		6.35		7,8
P	.100		2.54		
Q		.030		0.76	5
TL	.028	.048	0.71	1.22	3,4
TW	.036	.046	0.91	1.17	3
r		.010		0.25	10
α	45° TP		45° TP		6
1, 2, 9, 11, 12, 13					

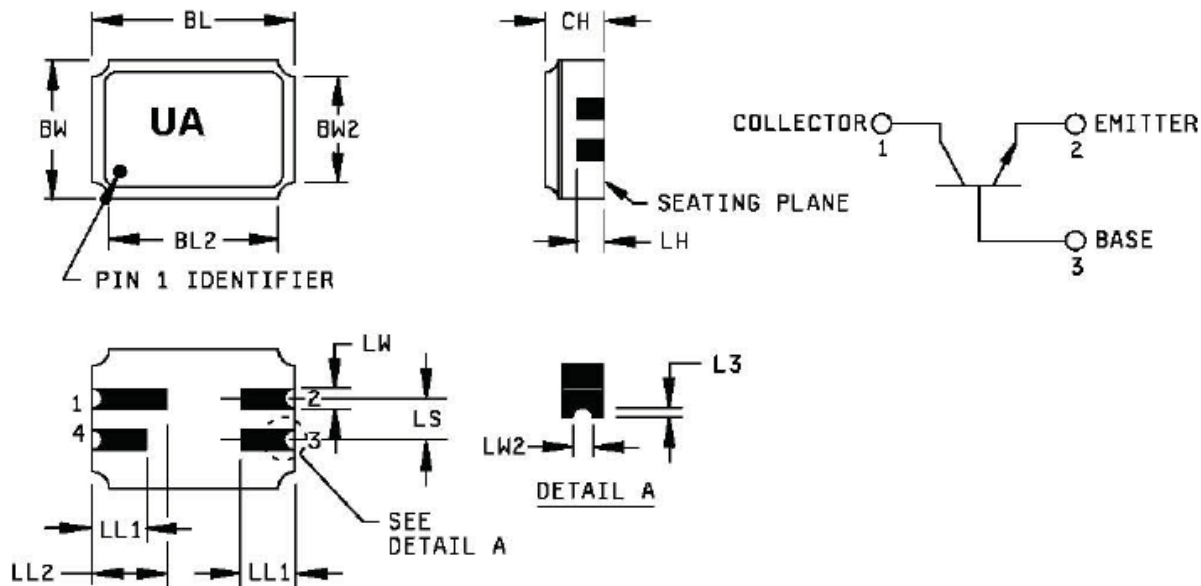
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Outline Drawing (UA Surface Mount)



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension CH controls the overall package thickness. When a window lid is used, dimension CH must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions LW2 minimum and L3 minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on the bottom two layers, optional on the top ceramic layer.) Dimension LW2 maximum and L3 maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. The co-planarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.215	.225	5.46	5.71	
BL2		.225		5.71	
BW	.145	.155	3.68	3.93	
BW2		.155		3.93	
CH	.061	.075	1.55	1.90	3
L3	.003	.007	0.08	0.18	5
LH	.029	.042	0.74	1.07	
LL1	.032	.048	0.81	1.22	
LL2	.072	.088	1.83	2.23	
LS	.045	.055	1.14	1.39	
LW	.022	.028	0.56	0.71	
LW2	.006	.022	0.15	0.56	5

Pin no.	1	2	3	4
Transistor	Collector	Emitter	Base	N/C

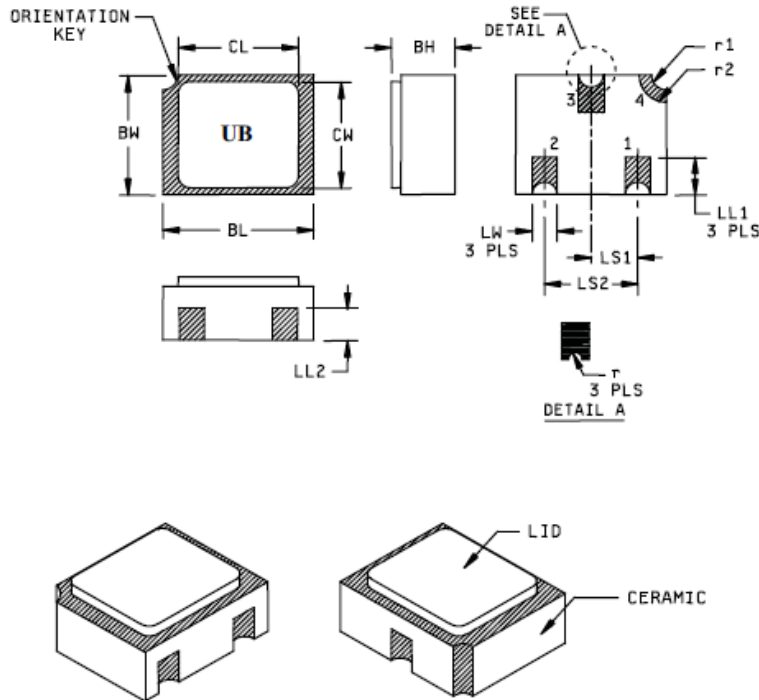
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Outline Drawing (UB, UBC* (*ceramic lid version) Surface Mount)



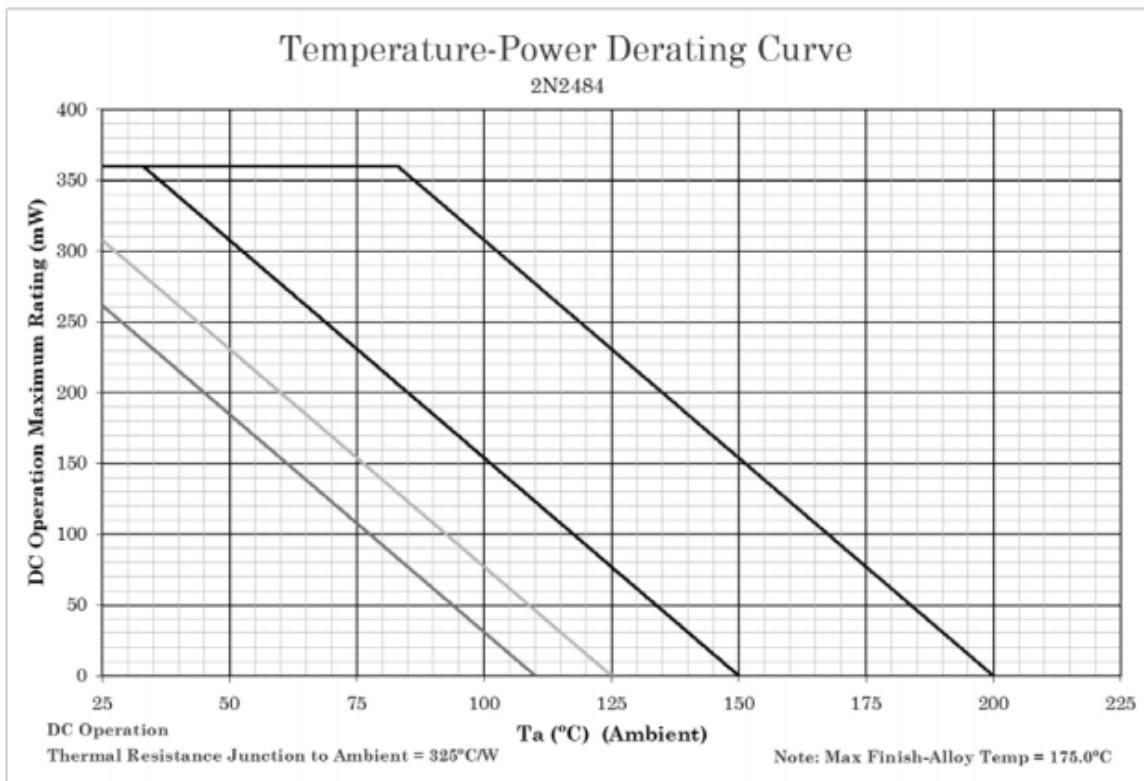
Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.046	.056	1.17	1.42	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.96	
LL2	.017	.035	0.43	0.89	

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
LS ₁	.036	.040	0.91	1.02	
LS ₂	.071	.079	1.81	2.01	
LW	.016	.024	0.41	0.61	
r		.008		.203	
r ₁		.012		.305	
r ₂		.022		.559	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metalized areas.
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

Temperature-Power Derating Curve

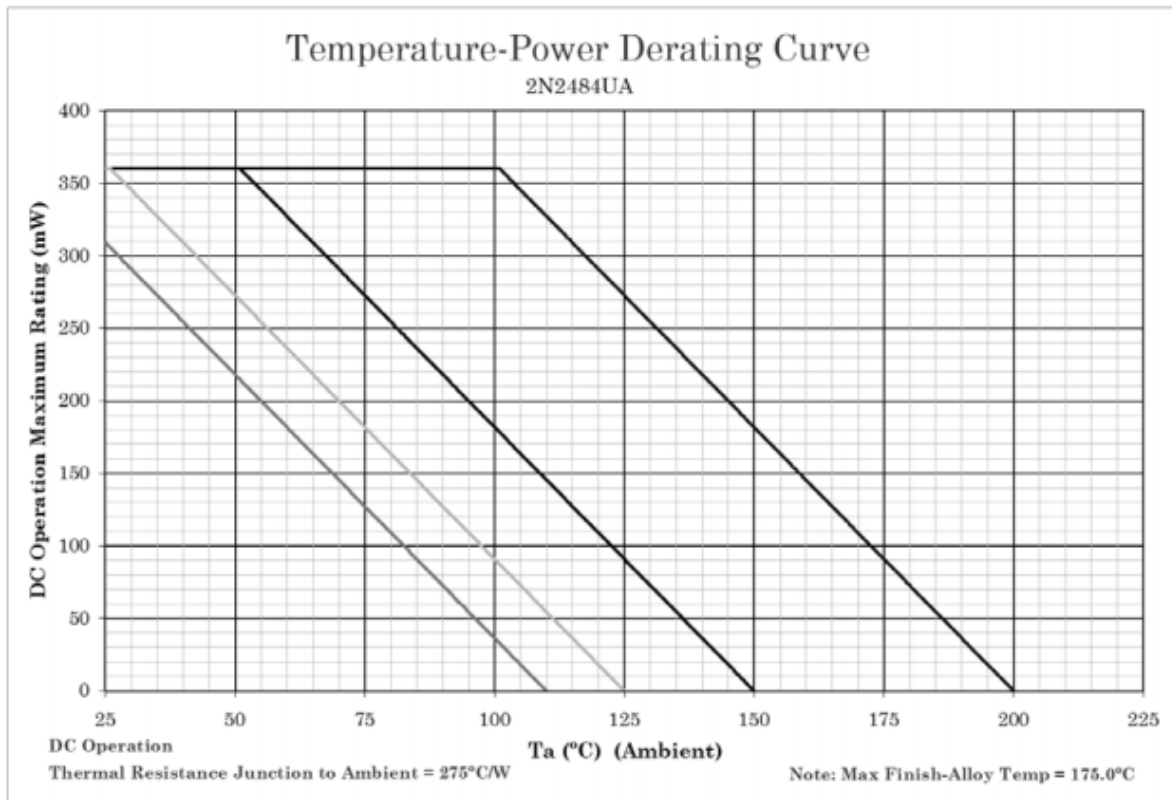


NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 7. Temperature-power derating for 2N2484, (TO-18 package).

Temperature-Power Derating Curve

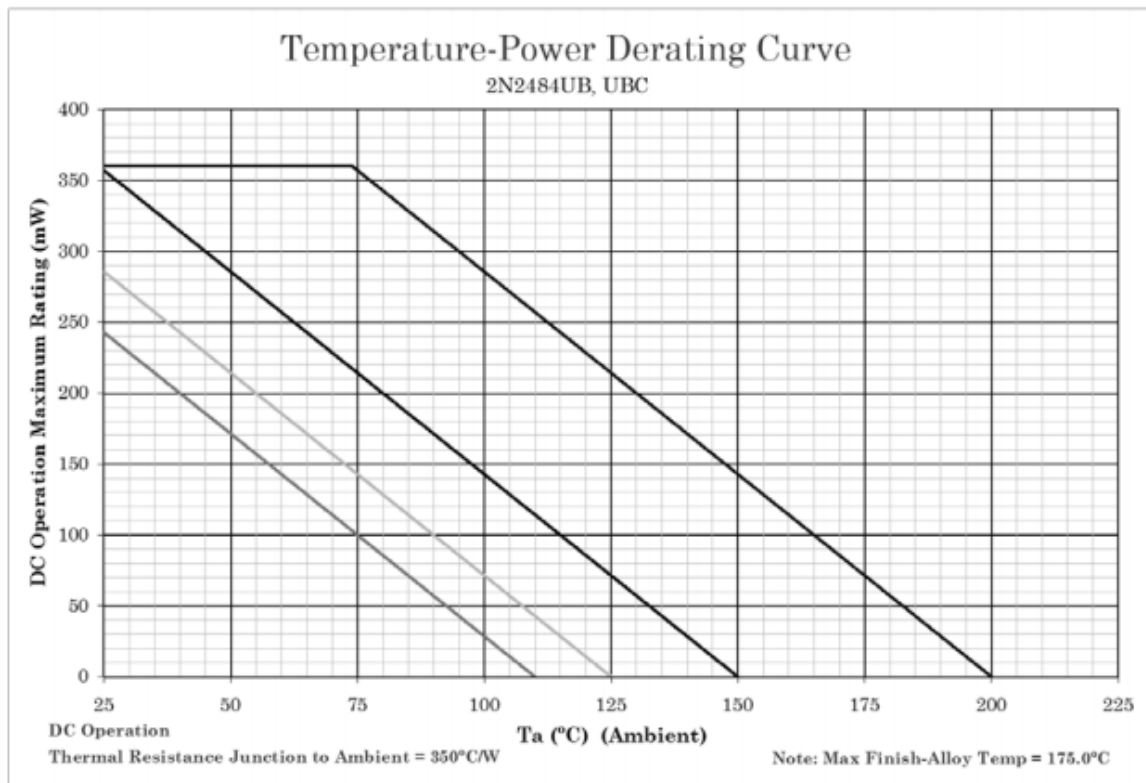


NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 8. Temperature-power derating for 2N2484UA, (UA package).

Temperature-Power Derating Curve



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 9. Temperature-power derating for 2N2484UB (UB, UBC, UBN, and UBCN package).

Thermal Impedance Curves

Maximum Thermal Impedance

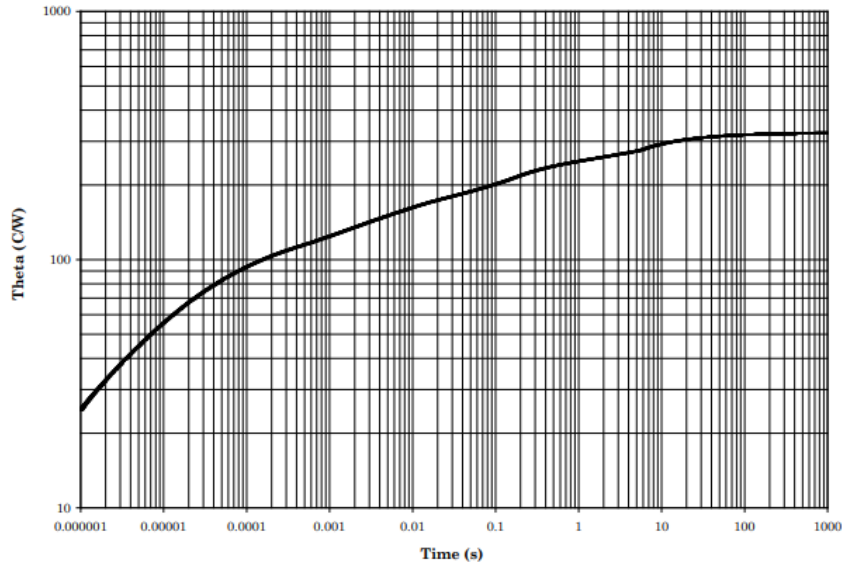


FIGURE 10. Thermal impedance graph ($R_{\theta JA}$) for 2N2484 (TO-18).

Maximum Thermal Impedance

LCC4 Package on FR4 PCB, Standard Bond Pads, $T_a=25^\circ\text{C}$, 360mW

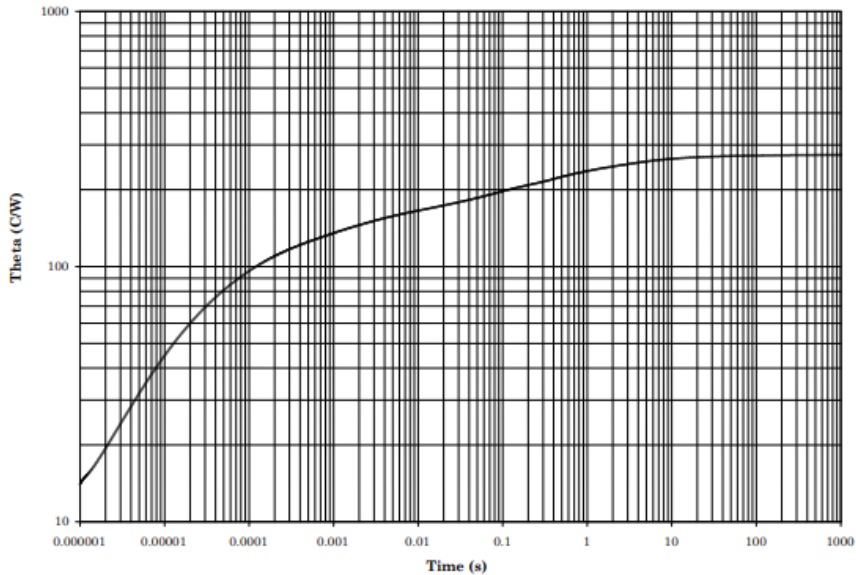


FIGURE 11. Thermal impedance graph ($R_{\theta JA}$) for 2N2484UA (UA).

Thermal Impedance Curves

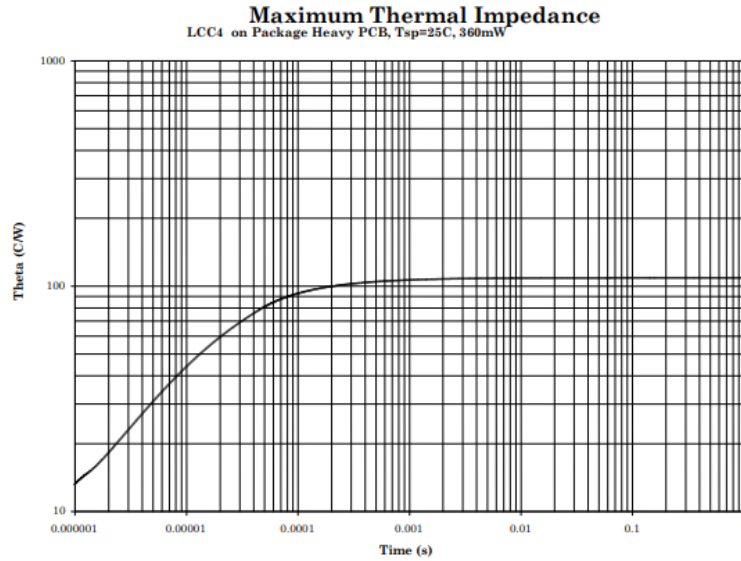


FIGURE 12. Thermal impedance graph ($R_{\theta JSP}$) for 2N2484UA (UA).

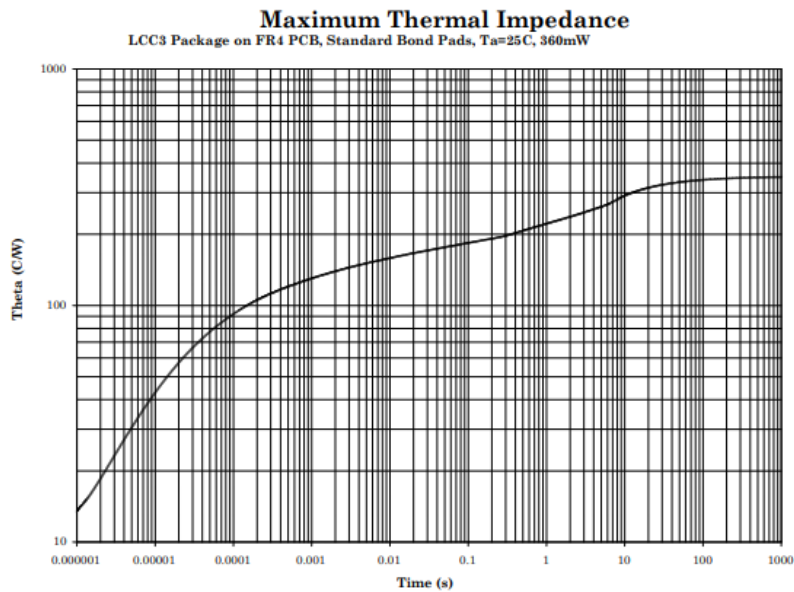


FIGURE 13. Thermal impedance graph ($R_{\theta JA}$) for 2N2484 (UB, UBC, UBN, and UBCN).

Thermal Impedance Curves

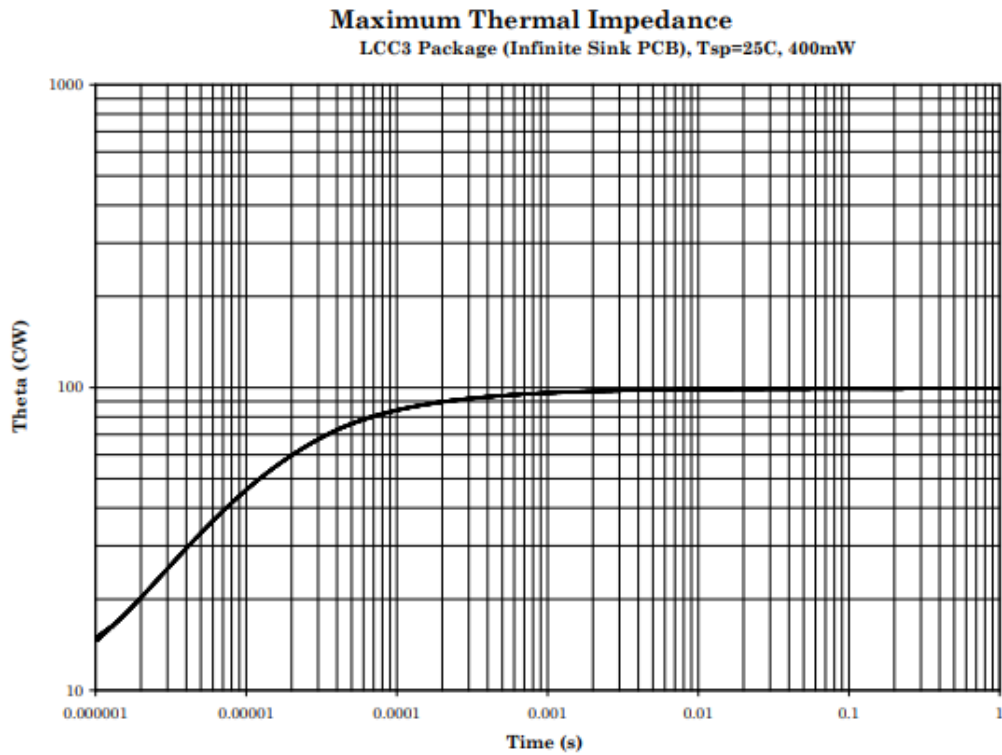


FIGURE 14. Thermal impedance graph ($R_{\theta JSP}$) for 2N2484 (UB, UBC, UBN, and UBCN).

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