VISHAY ELECTRO-FILMS

ES COMPONENTS
108 PRATTS JUNCTION
ROAD STERLING, MA 01564
PHONE: (978) 422-7641
FAX: (978) 422-0011
www.escomponents.com

An Introduction to Substrate PIMIC™ (Passive Integrated Microelectronic Interconnect Circuitry) Technology

Introduction

Thin film microwave integrated circuits have been evolving from a simple substrate medium which carries microwave/ RF or DC energy between active die to one which solves complex packaging problems including the reduction of discrete components, EMI management, packageless chip mounting, and the consolidation of digital and RF circuitry within a single assembly.

PIMIC™ technology (Passive-Integrated Microelectronic Interconnect Circuitry) has been developed by Vishay EFI technology to solve these unique problems by bridging the gap between ultra-high levels of silicon and GaAs integration and traditional chip and wire hybrid design approaches. Using a wide array of ceramic substrate materials and metal systems, combined with a kit of PIMIC™ design features and capabilities, the circuit designer can now easily reduce circuit size and parts count over traditional thin film substrate design approaches, simultaneously enhancing performance. Four levels of PIMIC™ technology, shown in cross-section in Figure 1, are offered by Vishay EFI Technology to meet a wide range of industry requirements and supported by completely captive high-volume fabrication capabilities.

In its simplest form, PIMIC-SI (Simple Interconnect) incorporates conductors, resistors, plated vias, and selective high conductivity traces for high-volume, low-cost, DC and RF products including standard microwave amplifiers and oscillators, cable TV circuitry, A/D converters, and high-power regulation.

PIMIC-AI (Advanced Interconnect) incorporates all passive elements in solid-state form. Microstrip conductors, resistors, inductors, capacitors, air-bridges, and filled thermal vias are integrated on a single substrate. Applications include highperformance, low-noise, and power amplifiers for use in commercial wireless products, avionics, and state-of-the-art T/R modules.

To address digital circuit requirements, PIMIC-HDDI (High-Density Digital Interconnect) substrates offer single or doublesided, controlled impedance signal routing. These MCM-D substrates also offer integrated resistors and solid thermal vias, if required, for improved performance. Applications include ASIC control circuits, highdensity memory modules, and digital switching networks.

By incorporating features of PIMIC-AI and -HDDI in a single design, EFI Technology has created PIMIC-MSI (Mixed Signal Interconnect) to address the expanding use of mixed technologies. This unique PIMIC™ process allows integration of analog and digital functionality for use in leading-edge, miniaturized military, satellite, and commercial electronics.

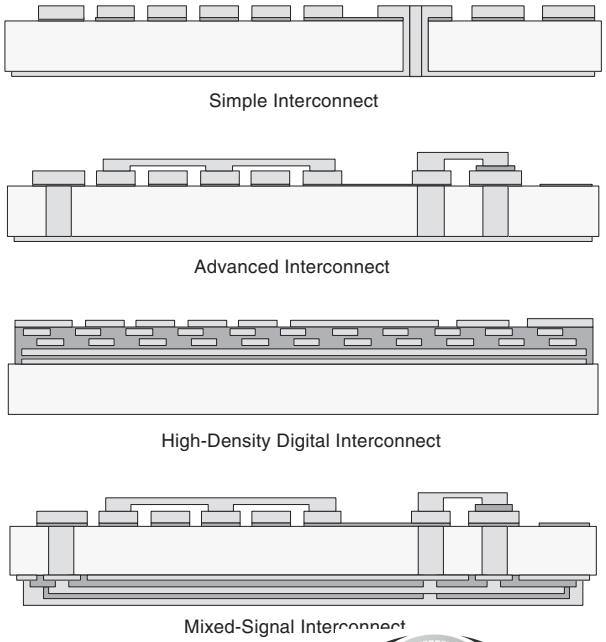


Fig. 1: PIMIC™ Pr

Using this

The Vishay EFI Technology P ide is a multisection document created to help our customers understand and design with PIMIC™ technology, while going about the design process in a logical manner. This introductory guide provides a roadmap for the design process, enabling the engineer to get started immediately on his or her design. The focus of this guide is on designs that meet standard specifications on high purity alumina or beryllia, while the single-subject brochures in EFIs complete Design Guide provide a higher level of detail for each PIMIC™ technology. The design process flow begins with the engineer choosing his or her level of PIMIC™ technology and then designing with the materials, features, and metal systems available within that category. Each PIMIC™ tool or feature identified in this brochure is linked to a defined number of PIMIC™ processes and materials, resulting in an extensive matrix of options. This wide selection of capabilities is constantly being developed and refined to meet the ever-growing needs of the electronic packaging industry. Special requests outside of the options detailed in this guide can be evaluated by your EFI sales engineer. The flow chart in Figure 2 illustrates the PIMIC™ design method.

TECH NOTE

An Introduction to Substrate PIMIC™ (Passive Integrated Microelectronic Interconnect Circuitry) Technology

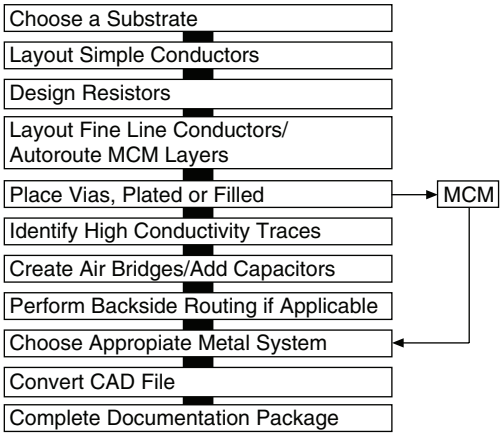


Fig. 2: PIMIC™ Design Flow

Step 1: Choosing a Substrate

The circuit engineer usually begins a circuit design by deciding on a substrate material and thickness. This process is particularly critical for high frequency designs where substrate dielectric constant and thickness have a significant impact on circuit size, performance, and dispersive effects. In addition to providing an ideal medium for microcircuit assembly, high dielectric constant ceramic materials such as alumina offer the advantages of reduced circuit size over teflon or polymer-based dielectrics. At even higher dielectric constant values, specialty ceramics offer smaller circuit sizes and make available, extremely low transmission line impedances.

Mechanical specifications including thermal conductivity (TC) and coefficient of thermal expansion (CTE) become critical parameters for high power designs where heat conduction and induced stresses are of concern. Materials including beryllia, aluminum-nitride, and quartz are often chosen for their function-specific mechanical properties. Common applications of these materials are detailed in Table 1.

Vishay EFI Technology has developed its fully integrated PIMIC^{TM} process around the most popular ceramic materials, namely alumina and beryllia. Various levels of PIMIC^{TM} integration are available on the other materials as a function of the demand for these products and their mechanical properties and process compatability. Table 2 summarizes the mechanical properties of the various substrate materials and the available level of PIMIC^{TM} processing. Special requests for PIMIC^{TM} processing not addressed in Table 2 can be handled by your local EFI sales engineer and factory representatives. In general, the designer should utilize as thick a substrate material as possible to simplify handling issues and reduce cost. For operating frequencies up to approximately 5 GHz, 25 mil (0.635 mm) material thickness is a logical choice. As operating frequency increases, the opportunity for waveguide-type transmission modes within the substrate develop, dictating thinner materials. Based upon past experience, Vishay EFI Technology recommends 15 mil (325 µm) through 18 GHz, 10 mil (250 µm) material to 44 GHz, and 5 mil material above 44 GHz. Thinner materials in general will reduce coupling of adjacent circuit structures, typically at the expense of narrower linewidths. The engineer should review his or her designs sensitivity to these issues.

Table 1 - Common Substrate Materials and their Applications

Alumina (Al_2O_8) 99.6 %	Low to medium power, DC/RF or Microwave circuits using Si or GaAs ICs	Cost-effective material with a wide range of applications
Beryllia (BeO)	High-power DC/RF/Microwave circuits using Silicon or GaAs JCs. High PowerTerminations	Extremely high thermal conductivity
Alluminum-Nitride (AIN)	High-power DC/RF/Microwave circuits using Silicon or GaAs JCs	Optimal CTE match with Silicon devices
Quartz (S_1O_2)	Microwave/Millimeter-wave circuits requiring extremely low loss or low CTE	Low Loss Tangent and CTE Smooth surface finish
Titanates	RF/Microwave amplifiers or oscillators requiring High-Q resonators and transformers	Dielectric constants available from 12 - 100
Ferrite Sapphire	RF/Microwave Circulators/isolators Millimeter-wave/optical circuits with special electrical or mechanical requirements	Magnetically activated material Low Loss Tangent Optical surface finish

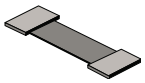
An Introduction to Substrate PIMIC™ (Passive Integrated Microelectronic Interconnect Circuitry) Technology

Table 2 - PIMIC™ Processes and Mechanical Properties by Material

Material	Processes	$\in_R$	Tan δ 1 MHz/10 GHz	Surface Finish (µ")	CTE (ppm/°C)	TC (W/M °C) 25C/100C	Common Thickness mils (mm)
Al_2O_3, 99.6 %	All	9.9	0.0001/0.0003	< 1 (pol) < 4 (a.f.)	7.0	35/27	5 -100 (0.125 - 2.5)
B_eO, 99.5 %	All	6.7	0.001/0.003	< 4 (pol)	7.6	290/240	10 - 100 (0.25 - 2.5)
AlN	SI, HDDI	8.9	0.0005/0.002	< 3 (pol)	4.5	170/130	10 - 100 (0.25 - 2.5)
Quartz	SI	3.8	0.00002/0.0001	60/40	0.55	5/2	10 - 40 (0.25 - 1.5)
Titanates	SI	12 - 100	> 0.0002	5 - 8 (pol)	varying	varying	10 - 60 (0.25 - 1.0)
Ferrite	SI	12 - 16	A > 0.0003	10	-	-	10 - 40 (0.25 - 1.0)
Sapphire	SI	9.3*/11.5**	0.00002/0.0001	60/40	5.3	40/30	10 - 40 (0.25 - 2.5)

*perpendicular to C-axis, **parallel to C-axis

Step 2: Designing Resistors



Applicability: SI, Al, HDDI, MSI

Assuming that a substrate material has been chosen and a simple conductor structure created, the design engineer may find a need to provide voltage division, current regulation, or power termination using thin film resistors. EFI Technologys thin film resistors are formed by lithographically patterning highresistance films of tantalum-nitride or nichrome deposited on the surface of a wide variety of substrate materials. In general, there are four parameters of concern to the engineer when designing a resistor: the resistor value, its change in value over time, its change in value with temperature, and its power handling capability. Secondary considerations include the choice of resistor material and sheet resistance. As with any type of resistor, total resistance is determined by the equation:

$$R = \rho L/Wt$$

Where:
R = Total Resistance ()
ñ = Bulk Resistivity of resistor material (Ωcm)
L = Resistor Length (cm)
W = Resistor Width (cm)
t = Resistor Thickness (cm)

With thin film resistors, sheet resistance in units of ohms per square (Ω) is often used to specify a film and resistor values are easily calculated based upon final resistor dimensions and sheet resistivity as follows:

R_{sheet} = Sheet resistance = ρ/t (Ω)
Where: = Unit Surface Area of Equal Length and Width
and: $R_{total} = R_{sheet}$ x Length/Width Ω)

Resistor parameters for alumina and several other substrate materials are identified in Table 3. For more information, consult Vishay EFI Applications Engineering. When laying out a rectangular, non serpentine resistor, a number of simple guidelines detailed in Table 4 should be followed. For more detailed information, including serpentine resistor requirements, resistor power handling, and dual resistivity capabilities, consult EFI's separate resistor guide.

Step 3: Designing Fine-Line Conductor Features

Applicability: SI, Al, MS

In its simplest form, a PIMIC-SI circuit employs resistors and conductors to interconnect and regulate DC signals. At RF frequencies, resonant structures or circuit elements employing fine-lines (< 2 mils) and spaces (< 1.5 mil) are oftenrequired along with the DC circuitry. Fine-line features are the speciality of thin film fabrication techniques, examples of which include Lange couplers, filters, interdigitated capacitors, and spiral inductors. The key to high-yield manufacture of these entities is proper material surface quality. The relatively coarse finish of beryllia, aluminumnitride, and titanates, even when polished, prevent linewidths below approximately 1.5 mils (37.5 µm) and spaces below 1 mil (25 µm) from being fabricated reliably. Polished alumina, however, with its excellent surface quality permits linewidths down to 0.6 mils (15 µm) and spaces down to 0.5 mils (12.5 µm) to be manufactured. The performance of many of these fine-line structures is adversely affected by adding wirebonds, so EFI Technology strongly recommends the use of airbridges to make solid-state interconnects as detailed later in this guide. Your EFI sales engineer can provide guidance on the proper choice of metal systems to achieve these fineline features as a function of substrate material, final geometry and product application.

An Introduction to Substrate PIMIC™ (Passive Integrated Microelectronic Interconnect Circuitry) Technology

Step 4: Lange Coupler Considerations

Lange Coupler Considerations: When designing a Lange coupler, the circuit engineer must consider operating frequency, substrate material, linewidths, spacings, and interconnection approach. EFI recommends airbridges on all Lange coupler designs to reduce wirebonding problems and the RF performance variations that result. Figure 3 shows a comparison of a simulated and measured data for an air-bridged Lange coupler. Several bridging methods exist to interconnect Lange fingers as illustrated in Figure 4. For lower input-impedance couplers, 6 or 8-finger Langes may be preferred over a 4-finger version. Finally, it is also important to watch for the the angle at which the RF transmission lines meet the Lange coupler fingers to prevent excessive neckdown at the finger/transmission line connection point as illustrated in Figure 4.

Table 3 - Standard Resistor Parameters

Material	TCR Range (ppm/°C)	Standard Sheet Resistivity, 99.6 % Alumina (Ω)	Standard Sheet Resistivity, BeO, AIN (Ω)	Stability	Tolerance
Tan	- 125 ± 25	25 - 125	25 - 100	< 0.5 %	0.5 - 10 %
NiCr	0 ± 25	50 - 250	50 - 150	< 0.2 %	0.1 - 10 %

Table 4 - Sample Resistor Layout-Guidelines

Parameter	Value inches (µm)	Comment
Resistor Style	Type-1	Resistor Inboard of Conductor
Min Resistor Dimension	0.002 x 0.002 (50 x 50)	
Min Probe Pad Dimension	0.003 x 0.003 (75 x 75)	
Conductor/ Resistor Overlap	0.0005 (12.5) per side 0.002 (50) per end	Perpendicular to current flow Parallel to current flow

Step 5 - Interdigitated Capacitors

This type of capacitor, shown in Figure 5, permits the designer to realize a planar capacitor up to several picofarads in value using closely spaced fingers, similar to a Lange coupler. A number of published articles referenced in EFIs guide to thin film capacitors detail closed form design equations for this type of capacitor as a function of width, spacing, number of fingers, and length. Microwave simulation tools including Touchstone and Super-Compact provide accurate library models for interdigitated capacitor analysis.

Step 6 - Spiral Inductors

High quality inductors are an essential part of manyamplifier and oscillator designs, or for broadband baluns and lumped element filters. EFI Technology manufactures circular or rectangular inductors as shown if Figure 5 using low loss metallization systems and other techniques to create structures with higher Qs (50 min at 10 MHz) than are available on GaAs or silicon. Linewidths and spacings down to 0.0005 (12.5 µm) are possible although most requirements can be met with 1.5 mil lines and 1 mil spacings. Furthermore, wider spacings permit the use of conductors up to 1 mil (25 µm) thick for even lower loss characteristics. Finally, air-bridges to the center-tap of spiral inductors (addressed later in this guide) result in a reduced bond count, highly reliable assembly.

An Introduction to Substrate PIMIC™ (Passive Integrated Microelectronic Interconnect Circuitry) Technology

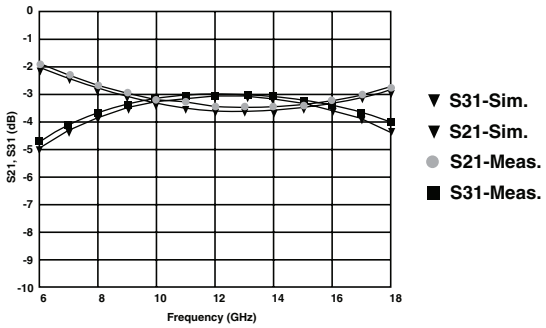


Fig. 3: Typical Air-Bridge Lange Coupler Perfromance

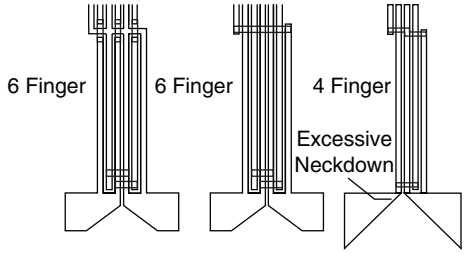


Fig. 4: Typical Lange Coupler Layout Approaches

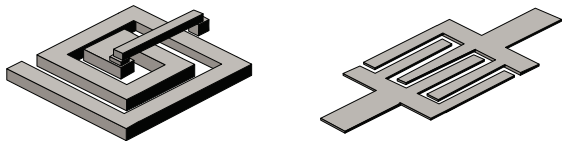


Fig. 5: Typical Spiral Inductor and Integrated Capacitor

Step 7 - Designing Plated Via Holes

Most circuit designers quickly discover the convenience of implementing connections to the backside ground-plane of their circuit through the use of metallized via holes. EFI Technology offers these plated holes on a full range of substrate materials using the sizing guidelines of Table 5. For those circuit designers unable to take advantage of the benefits of filled vias because of ongoing programs or designs which are under configuration control, plated vias from EFI Technology provide a mature process option with high reliability. Designers wishing to update their plated viacircuits to use filled vias may also do so with no conductor trace design changes. With any filled via circuit, however, all vias must be filled, rather than just a selected portion. Consult your EFI sales engineer for assistance in upgrading your circuit to use filled vias. Further information is included in EFIs Applications and Design of Plated & Filled Via Circuits Guide.

Table 5 - Plated Via Design Parameters

Substrate Height Inches (mm)	Filled Via Diam. Inches (mm)	Capture Pad Dimension Inches (mm)	Via Spacing Center to Center Inches (mm)	Via Spacing Center to Circuit Edge Inches (mm)
0.005 (0.125)	0.007 - 0.02 (0.175 - 0.500)	Diam + 0.010 (Diam + 250)	Diam + 0.02, 0.03 min (Diam + 0.05)	Diam/2 + 0.02 (Diam/2 + 0.5)
0.010 (0.250)	0.007 - 0.04 (0.175 - 1.0)	Diam + 0.010 (Diam + 250)	Diam + 0.02, 0.03 min (Diam + 0.05)	Diam/2 + 0.02 (Diam/2 + 0.5)
0.015 (0.375)	0.009 - 0.10 (0.225 - 2.5)	Diam + 0.010 (Diam + 250)	Diam + 0.02, 0.03 min (Diam + 0.05)	Diam/2 + 0.02 (Diam/2 + 0.5)
0.020 (0.500)	0.012 - 0.10 (0.300 - 2.5)	Diam + 0.010 (Diam + 250)	Diam + 0.02 (Diam + 0.05)	Diam/2 + 0.02 (Diam/2 + 0.5)
0.025 (0.625)	0.015 - 0.15 (0.375 - 3.75)	Diam + 0.010 Diam + 250)	Diam + 0.02 (Diam + 0.05)	Diam/2 + 0.02 (Diam/2 + 0.5)

Note: A barrier metal on the backside of the circuit may be required when using plated vias.

Table 6 - Filled Via Layout Parameters

Substrate Thickness Inches (mm)	Filled Via Diam. Inches (mm)	Filled Via Material	Substrate Material	Via Spacing Center to Center Inches (mm)	Min. Capture Pad Size Inches (mm)	Via Spacing Center to Circuit Edge
0.010 (0.250)	0.006 (0.15)	Au, Cu	Al_20_3, BeO, AlN	0.012 (0.30)	0.011 (0.279)	0.009 (0.230)
0.010 (0.250)	0.014 (0.35)	Au, Cu	Al_20_3, BeO, AlN	0.028 (0.71)	0.019 (0.475)	0.021 (0.533)
0.015 (0.375)	0.008 (0.20)	Au, Cu	Al_20_3, BeO, AlN	0.016 (0.40)	0.013 (0.330)	0.012 (0.304)
0.015 (0.375)	0.014 (0.35)	Au, Cu	Al_20_3, BeO, AlN	0.028 (0.71)	0.019 (0.431)	0.021 (0.533)
0.020 (0.500)	0.010 (0.25)	Au, Cu	Al_20_3, BeO, AlN	0.020 (0.25)	0.015 (0.381)	0.015 (0.383)
0.020 (0.625)	0.020 (0.50)	Au, Cu	Al_20_3, BeO, AlN	0.040 (1.0)	0.025 (0.625)	0.030 (0.750)

An Introduction to Substrate PIMIC™ (Passive Integrated Microelectronic Interconnect Circuitry) Technology

Step 8: Designing With Filled Vias

Applicability: Al, MSI, HDDI

EFI Technologys filled via process has overcome all of the limitations of plated-through holes and brought new flexibility to the module or circuit designer. Filled vias provide a planar, low resistance microwave grounding path, allowing high performance silicon and gallium-arsenide RF circuits to be surface mounted on PIMIC™ substrates. Assembly concerns are removed by eliminating epoxy and solder bleed problems, while the high thermal conductivity of filled vias provide a cooling path for high-power active die. Finally, surface-mount packaging applications benefit from EFIs filled vias as I/O connections. Table 6 provides fundamental layout information while the Plated and Filled Via application guide further discusses modeling and mechanical parameters.

Step 9: Designing High Conductivity Traces

Applicability: SI, Al, MSI

EFI Technology has developed the unique capability to manufacture selective, high conductivity traces on PIMIC substrates to reduce resistive losses in high-current lines. Conductor traces have a measurable resistance due to the cumulative resistances of each of the metals used. As with resistors, sheet resistance (in mΩ) are the typical unit of resistance measurement. For circuit traces carrying highcurrents (100s of mA) over large distances (100s or 1000s of mils), the resistive losses of a narrow line can become significant, resulting in reduced voltages at the terminals of FETs or other active circuit elements. By increasing the thickness of selected high-current lines, the engineer may now have fine-line RF structures such as Lange couplers on the same circuit with low-loss DC lines. As line thickness increases, however, minimum linewidths and tolerances also increase slightly. Tables 7 and 8 identify selected sheet resistances and standard high conductivity metallization options. Check the metals selection portion of this guide for metal system compatability with high conductivity coatings.

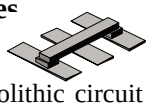
Table 7 - High Conductivity Metal Systems

Metal Options	Typical Metal Layers	Minimum Lin/Tol. (mils)
Copper (100 - 6000 µ")	TiW (500 - 1000 A)	N/A
	Au (100 - 150 µ")	0.6 / 0.1
	Cu (2200 ± 400 µ")	5.0 / 0.5
	Ni (80 - 250 µ")	5.0 / 0.5
	Au (100 - 200 µ")	5.0 / 0.5
Gold (500 - 4000 µ")	TiW (500 - 1000 A)	N/A
	Au (100 - 150 µ")	0.6 / 0.1
	Au (300 - 850 µ")	3.0 / 0.3

Table 8 - Selected Sheet Resistives

Metal	Thickness	Sheet RSheet mΩ
Au	150 µ"	7 - 8
	600 µ"	2.0
Cu	2000 µ"	0.21

Step 10: Designing Air-Bridges



Applicability: Al, MSI

Air-bridges have long been used in the monolithic circuit world for connecting FETs, capacitors, and transmission lines to other parts of a circuit network. For nearly a decade, EFI Technology has been applying the same air-bridge technology to the manufacture of thin film ceramic circuitry, enabling circuit designers to eliminate bond wires. Fine-line structures, such as Lange couplers, have continued to push downward in size as frequencies and bandwidths have increased resulting in couplers that are too small to be bonded reliably. Because of this, airbridges are a critical addition to any Lange coupler having geometries at or below 0.0025 (62.5 µm). Properly designed and manufactured bridges have no impact on RF performance, also making them ideal for retrofitting older, wirebonded designs. Furthermore, encapsulation of these structures makes them highly reliable throughout the assembly process.

Step 11: Air-Bridge Design Rules:

Refer to Figure 6 and Table 9.

1) Create 3 CAD layers on your design system:
   CONDUCTOR = Base conductor level
   AB = Air-Bridge metallization
   POLY = Polyimide insulators
2) Create the required base level conductor geometry on the CONDUCTOR layer. This might include such structures as a Lange coupler, spiral inductor, or even a simple DC crossover site.
3) Create the air-bridge on the AB layer, conforming to the width and overlap requirements.
4) Create the insulator layer under the air-bridge using a rectangle on the POLY layer. This insulator layer is not necessary for short air-bridges and may be deleted at EFIs discretion.
5) For encapsulated air-bridges, add an additional rectangle on the POLY layer to define the protected region.
6) Review the aspect ratio of the unsupported portion of the air-bridge. When designing your air-bridge, careful attention should be paid to this length/width aspect ratio to ensure that it is no more than 6:1.Widen or shorten the bridge as required.

An Introduction to Substrate PIMIC™ (Passive Integrated Microelectronic Interconnect Circuitry) Technology

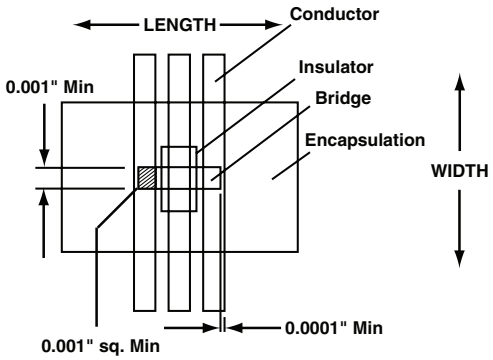
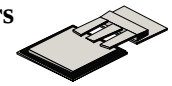


Fig. 6: Typical Air-Bridge Design

Step 11: Thin Film Capacitors



Applicability: Al, MSI

EFI Technologys thin film capacitors are constructed using a Metal-Insulator-Metal approach with either a silicon-nitride or polyimide dielectric, and gold electrodes. Connections between the capacitor and adjacent thin film circuitry are made using air-bridges. This approach to capacitor construction is in contrast to other available technologies including discrete chip capacitors manufactured using singlelayer or multi-layered, high dielectric ceramics and attached to base circuitry using epoxy, solder, and wire bonds. The resultant capacitors have the advantage of small size, high Q, and reduced assembly. Table 10 highlights a number of important electrical and mechanical properties of these capacitors. A typical silicon-nitride capacitor layout is also illustrated in Figure 7. Clearly defined layout guidelines are detailed in the Applications and Design of Thin Film Capacitors Guide. Alternate design approaches including capacitors over filled vias as well as interdigitated styles are also discussed.

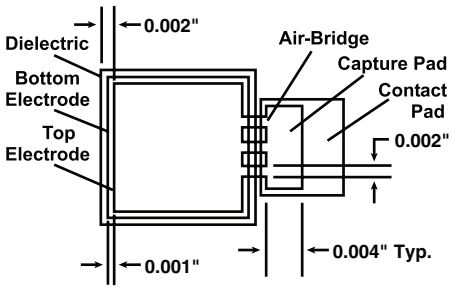


Fig. 7: Typical Silicon-Nitride Capacitors Layout

Step 12: Using Ground-Signal-Ground

Applicability: Al, MSI, HDDI

The increased use of mixed-signal circuit designs combining rapidly switched digital control signals or power supply signals with RF/microwave circuitry creates a hostile crosstalk environment within complex electronic assemblies. EFI Technology has developed ground-signal-ground (GSG) multilayer technology for use on PIMIC-Al and PIMIC-MSI circuits to solve this problem. This unique process enables the routing of shielded signals on the backside of PIMIC™ circuits without disrupting RF ground plane continuity. For ease of use, EFI Technology provides low cost autorouting and artwork generation for backside GSG layers, from an initial customer design which includes the front side circuit layout and a connection netlist. A typical application of this product is within a densely packaged microwave module where FET bias connections and control lines run in close proximity to microwave transmission lines. High current pulses on the drain lines or rapidly switching modulation signals can induce significant noise on adjacent conductor traces. Using ground signal-ground technology, the circuit engineer routes noisy high-current traces or sensitive bias/control lines on the back side of the substrate while complex RF structures such as air bridged Lange couplers coexist on the top side of the circuit. Filled vias are used to connect these signals to the appropriate points on the top side of the circuit. Metal layers on the circuit backside combined with polyimide insulators and special grounding techniques ensure electrically isolated signal lines without disruption of the RF ground plane. A detailed description of design rules is included in the Mixed-Signal Circuit Design Using Ground-Signal-Ground Technology Application Guide for those customers that desire to generate their own layouts. Basic properties of this technology are detailed in Figure 8 and Table 11.

An Introduction to Substrate PIMIC™ (Passive Integrated Microelectronic Interconnect Circuitry) Technology

Table 9 - Air-Bridge Design Rules

Parameter	Minimum Value mils (µm)	Comment
Bridge Width	1.0 (25)	0.1 mil Bridge to conductor pullback
Bridge/Conductor Overlap	1 mil^2 (645 μm^2)	-
Bridge Length	3.0 (75)	Minimum
Insulator Dimension	1.5 (37.5) Length, 3.0 (75) Width	0.1 mil min Insulator to Conductor Overlap
Encapsulation	Bridge Width + 6 (150) Bridge Length + 8 (200)	Minimum
Bridge Height	0.35 (8 µm)	Minimum
Bridge Thickness	0.225 (5.1 µm)	Minimum supported
Aspect Ratio	1:6	Unsupported Area, Recommended

Table 10 - Thin Film Capacitor Specifications

Parameter	Silicon-Nitride Capacitor	Polymide Capacitor
Dielectric Constant	7.8	3.2
Dielectric Thickness	2600 Å	5 µm
Capacitance Density	0.15 pf/mil^2 (233 pf/mm^2)	0.0031 pf/mil^2 (5.66 pf/mm^2)
Standard Values	10 - 100 pf	0.5 - 50 pf
Standard Tolerances	10 % (> 50 pf) 20 % (< 50 pf) 20 % Tighter Tolerances Available	20 % Special Tolerances Available
Circuit Connection	Encapsulated Air-Bridges	Encapsulated Bridges
Breakdown Voltage	50 V Min.	5 V Min. (1 V/µm)

Table 11 - Mechanical Characteristics of Ground-Signal-Ground

Parameter	Value	Description
Substrate Material	Alumina BeO	10 - 25 mils thick 15 - 25 mils thick
Layers, Front Side	1 - 6	Resistors, Conductors, Capacitors, Air-Bridges
Layers, Back Side	5	M1 = M3 = Ground P1 = P2 = Insulator M2 = Signal
Interconnection Method, Front to Back	Filled Vias.	Compliant to Requirements of Via Spaces
Conductor Sheet Resistance	5 mΩ/sq	Typical

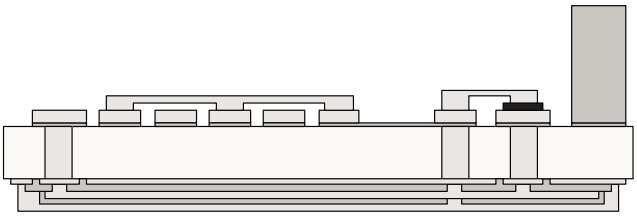


Fig. 8: Typical Ground-Signal-Ground Circuit Cross-Section

An Introduction to Substrate PIMIC™ (Passive Integrated Microelectronic Interconnect Circuitry) Technology

Table 12 - High Density Digital Interconnect Substrate Parameters

Parameter	Value	Comment
Substrate Type	Alumina, BeO, AlN	
Conductor Material	Gold	
Dielectric Material	Polyimide	
Dielectric Thickness	10 µm/5 µm	GND to PWR/X to Y
Dielectric Constant	3.2	
Number Of Conductor Layers	2 - 6	
Line Impedance	25 - 75 Ω	per design requirements
Line Width, Typical	2 mil (50 µm)	1 mil (25 µm) available
Line Spacing, Typical	2 mil (50 µm)	1 mil (25 µm) available
Sheet Capacitance, X-Signal	0.005 pF/mil^2 (0.8 nF/cm^2)	Typical
Sheet Resistivity	5 mΩ	Typical
Via Resistance	< 2 mΩ	Typical
Via Diameter	3 mil (75 µm)	2 mil (50 µm) available
Other Features	Filled Substrate Vias, Thin Film Resistors	

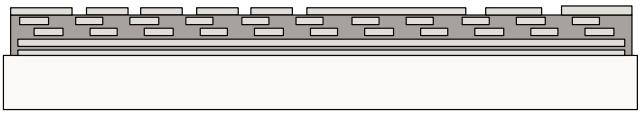


Fig. 9: MCM Cross-Section

Step 13: Applying High-Density Interconnect

Applicability: MSI, HDDI

High-density digital interconnect circuits, also known as MCMD substrates provide a dense packaging solution for chip and wire or flip-chip digital systems as well as mixed-signal products. EFI Technology utilizes a thin film on ceramic technology with a polyimide/gold insulator/conductor system similar to the ground-signalground system described in the previous section. Furthermore, EFI Technology can selectively apply the HDDI process to the front or back of RF/microwave substrates requiring digital functionality to yield a mixed-signal interconnect circuit. Using anywhere from 2 to 6 conductor layers, EFIs HDDI technology enables high-density generic or function-specific interconnect layers. For reduced cost, low clock rate designs, engineers typically route signal and power on unsegregated layers to achieve a lower final layer count. For higher speed designs, requiring optimal power and ground plane distribution and well controlled line impedance, EFI offers a standard ground/power/signal topology consisting of up to 6 functionspecific conductor layers. Other high performance low-cost MCM topologies, published in the literature, are also available using the same base process capabilities. Fully automated testing is applied to the completed design using a highspeed prober and a customer netlist. EFI Technology will also autoroute your design from a variety of netlist formats using state-of-the-art autorouting CAD tools. Figure 9 illustrates a 5 layer MCM cross-section on alumina, while Table 12 details baseline HDDI design parameters.

Step 14: Choosing your Metal System

Applicability: SI, Al, MSI, HDDI

EFI Technology offers over 20 metal systems to suit the needs of our customers. For PIMIC-SI circuits, the customer enjoys the most flexibility in choice of metal system due to the simpler process requirements of these products. As the complexity of any design increases, the menu of available metal systems necessarily narrows to fewer choices to enable process control and high yield. Each metal deposited on the surface of a substrate material as part of a complete system serves one or more specific purposes, namely that of resistor, adhesion, barrier, or conductor. Table 13 identifies the specific functions of the available metals as well as their desirable thickness ranges. At this point in your design, a metal system may be chosen as a function of the PIMIC™ integration level employed in your design as well as the assembly requirements of the final product, namely solder media and wirebonding. Generally speaking, the high solubility of gold in lead-bearing solders requires additional barrier metals in the metal system to ensure reliable device attachment. Furthermore, to limit solder joint embrittlement, gold thicknesses should be limited to a maximum of 100 microinches (2.5 µm). Conversely, for gold bearing solders, thicker gold layers are desirable and barrier metals are optional. Temperature limitations for different metal systems are also an important consideration to prevent intermetallic formation at the layer boundaries as well as to limit the potential for surface oxide growth due to barrier metal migration. All of the thin film metal systems offered by EFI Technology are readily bonded using gold wire. For optimal bond integrity, a minimum of 100 microinches gold thickness is recommended although reasonable bonding results can be achieved down to 50 microinches. Table 14 provides a matrix of PIMIC™ process and assembly options. Additional metal system capabilities are available at EFI Technology subject to review by our sales engineers or factory representatives. EFI welcomes inquiries on these nonstandard systems and guarantees a prompt and careful review of your requirements.

An Introduction to Substrate PIMIC™ (Passive Integrated Microelectronic Interconnect Circuitry) Technology

Table 13 - Metals and their Functions

Material Function	Types of Materials	Range of Values	Comments
Resistor	Tantalum-Nitride (TaN)	10 - 150 Ω (max)	25 - 125 Ω (Std)
	Nickel-Chromium (NiCr)	25 - 250 Ω (max)	
Adhesion	Titanium-Tungsten (TiW)	250 - 1000 Angstroms	Ideal for High Temp.
	Chromium (Cr)	250 - 750 Angstroms	LowTemp. Limitation
Barrier	Nickel (Ni) - Sputtered	750- 1500 Angstroms	Standard Barrier
	Nickel (Ni) - Plated	40 - 100 µ" (1 - 2.5 µm)	High Conductivity Barrier
	Palladium (Pd)- Sputtered	750 - 1500 Angstroms	Minimum 2 mil Features
	Platinum (Pt)	250 - 750 Angstroms	B-Side Only
Conductor	Gold (Au)	100 - 200 µ" (0.4 - 5 µm)	Tight Tolerance, Fine
High Current Conductor	Copper (Cu)	100 - 200 µ" (0.4 - 5 µm)	Line Features Available
	Gold (Au)	400 - 1000 µ" (10 - 25 µm)	3 mil Traces, 0.3 mil Tol.
	Cu/Ni/Au	1.5 - 4.0 mils (37 - 100 µm)	5 mil Traces 0.5 mil Tol.

Table 14 - Metal Systems and their Applications

Metal System	PIMIC™ Process	Bondable Gold Wire	Solderable, Lead Bearing (5)	Solderable, Gold Bearing (6)	Fine Lines (< 1.5mils)	Max Temp
Cr/Au (2)	SI	Y		Y	Y	300
Cr/Cu/Au	SI	Y	Y			300
Cr/Au/Cu/Au	SI	Y	Y			300
NiCr/Cu/Ni/Au (1)	SI	Y	Y	Y		350
NiCR/TiW/Cu	SI		Y			250
NiCR/Ni/Au	SI	Y	Y	Y		350
TaN/TiW/Au (2)	All	Y		Y	Y	450
TaN/TiW/Ni/Au	All	Y	Y	Y		350
TaN/TiW/Pd/Au	SI, AI	Y	Y	Y		400
TiW/Au (2)	.All	Y		Y	Y	450
TiW/Cu/Au	SI	Y	Y			300
TiW/Ni/Au	All	Y	Y	Y		350
TiW/Au/Ni/Au (1)	All	Y	Y	Y	(4)	350
TiW/Pd/Au	SI, AI	Y	Y	Y		400
TiW/Pt/Au (3)	SI	Y	Y	Y		450

Notes: (1) Thick Plated Nickel
(2) Selective Cu/Ni/Au Available For Loss Or Bump Mounting
(3) B-Side Only
(4) Selective Fine-lines
(5) Gold < 100 microinches
(6) Gold > 100 microinches

An Introduction to Substrate PIMIC™ (Passive Integrated Microelectronic Interconnect Circuitry) Technology

Step 15: Laser Features and More

Applicability: SI, Al, MSI, HDDI

A variety of other capabilities are available from EFI technology in conjunction with PIMIC™ products, including laser machined cutouts and profiling, edge-wrap metallization, two-sided patterning, and selective passivation/ solder dam using Si_3N_4 or polyimide.

Laser Machining:

For customers requiring laser machined cutouts in their circuits, EFI Technology provides complete in-house laser machining capabilities. This capability is useful for substrates assembled into odd-shaped housings or for extremely highpower active die being soldered to a housing floor. Table 15 highlights mechanical tolerances and guidelines for designing cutouts while further examples are detailed in the layout guide at the back of this publication.

Edge-Wrap Metallization:

Edge-wrap etallization, and castellations in the form of halfvias and halfslots are not recommended by EFI Technology due to their inferior mechanical strength compared to filled or plated vias. If your circuits require this technology because of ongoing programs under configuration control, EFI welcomes designs which meet the rules outlined in the layout guidelines reference page.

Selective Passivation/Solder Dam:

Circuits requiring passivation or solder dam may utilize EFI Technologys inhouse Si_3N_4, or polyimide insulator capabilities. In most instances a thin (2000 A°) layer of Si_3N_4 is the preferred choice. If it is a solder dam that is needed a selective layer (500 A°) of TiW is the preferred low cost approach. Alternatively, circuits making use of selective NiAu metalization may have the gold removed inselective areas to provide a nickel oxide solder dam.

Gold Tin Solder Layer:

A spattered 2-8 micron layer of AuSn (80/20) solder may be applied to conductor surfaces. Table 16 below highlights the features and design guidelines.

Table 15 - Laser Machining

Parameter	Value	Comment
Substrate Types	Alumina, BeO, AlN, Quartz, Titanates	
Pullback From Circuit Edge	0.02"	Minimum
Tolerance	± 0.003"	± 0.002" available
Corner Radius	0.006"	Minimum
Aspect Ratio, Remaining Material	5:1	Recommended

Table 16 - AuSn Solder

Parameter	Value	Comment
Substrate Types	Alumina, BeO, AlN, Quartz, Titanates	
Minimum Feature Size	0.002" x 0.002"	
Material Composition	80/20 AuSn	
Melting Point	280 °C	
Thickness	2-8 Micron	8 Micron standard
Pullback From Conductor	0.0005"	Minimum

Step 16: High Volume/Low Cost Applications

The evolving requirements for high density interconnects has driven EFI Technology to offer a high volume manufacturing capability to answer our customers needs for cost effective solutions. EFI Technologys increasing portfolio of capabilities offers the designer a wide flexibility for meeting the demands of todays markets. Applications in the markets of wireless and fiber optic telecommunication, CATV, medical, and military systems are readily solved using EFI Technologys array of design features. For more information including design rules, consult EFIs separate guide Cost-Effective High Volume interconnect Solutions. It should be noted that an EFI Technology sales engineer should work closely with the designer to ensure the most cost effective solution.

An Introduction to Substrate PIMIC™ (Passive Integrated Microelectronic Interconnect Circuitry) Technology

Step 17: Customers Inputs

To properly initiate an order with EFI Technology, customers are requested to provide the following information:

Inputs:

- Mechanical drawings including critical dimensions, tolerances, and component values.
- CAD files to finished dimensions using zero-width polylines.
- A Factory Approved Metallization System per PIMIC™ design rules.
- Assembly, Quality, and Environmental requirements.
- Netlist and Specific Probing Requirements for multilayer, GSG, or MSI circuits.

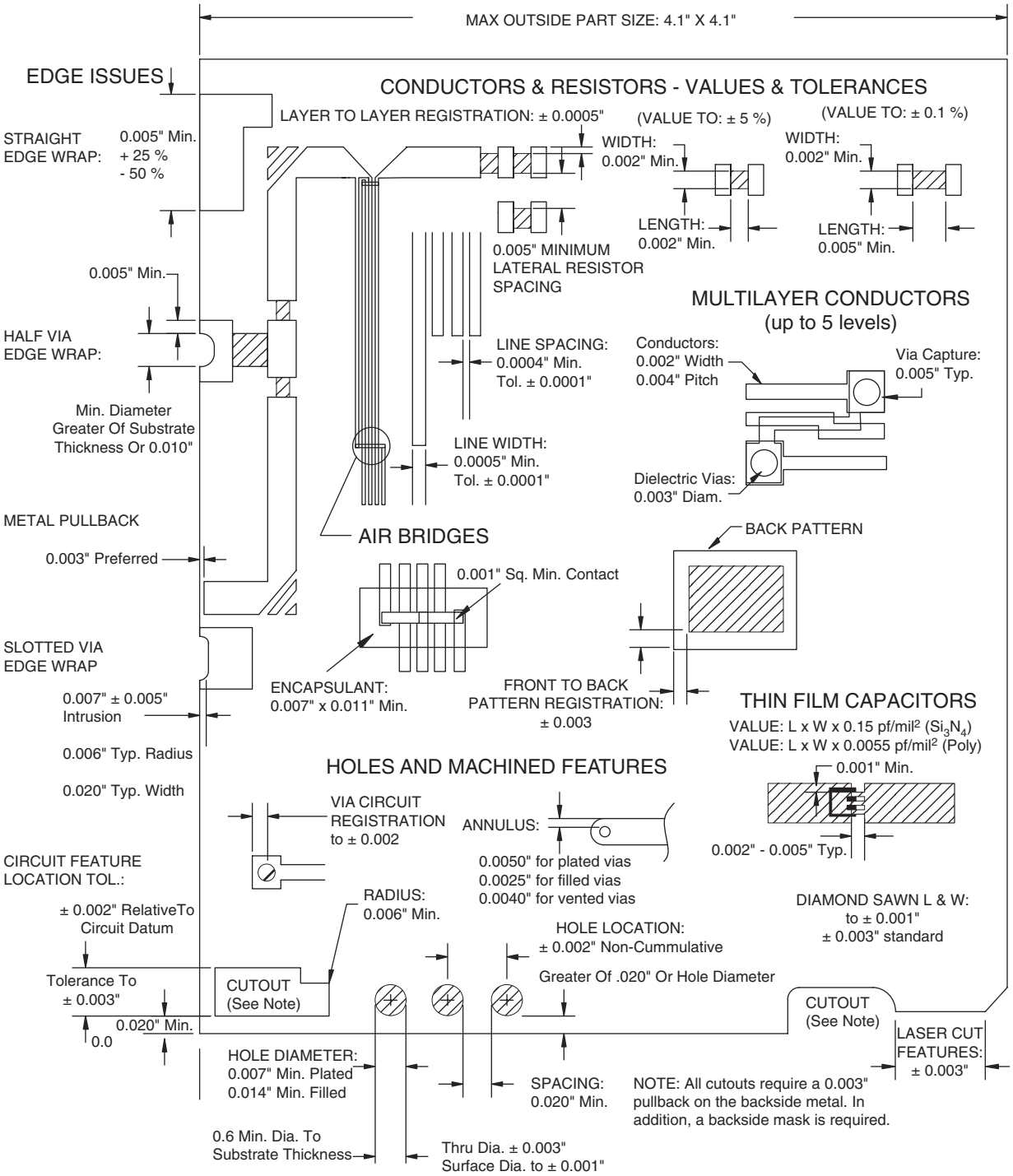
To speed your order, the preferred file formats are DWG and DXF. Circuit features should ideally be constructed using closed polygons and zero width polylines as noted above. Electronic transfer services including E-mail and modem are available to simplify entry of your order.

Step 18: Quality

EFI Technology products are guaranteed to meet or exceed all applicable military quality standards including MIL-STD- 883D, Method 2032, Class H. Class K testing for space requirements is also available as required. All tests are performed in house. Furthermore, EFI Technology guarantees that you will be 100 percent satisfied with our products and that they will function per your requirements.

An Introduction to Substrate PIMIC™ (Passive Integrated Microelectronic Interconnect Circuitry) Technology

Standard Layout Guidelines



TECH NOTE