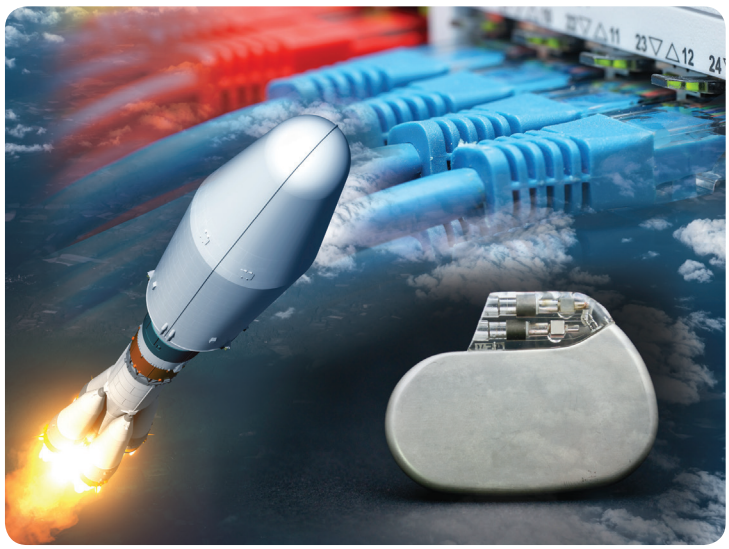
Thin Film Design Guide for Custom Substrates



This guide provides a roadmap for the design process covering the following information:

- Choosing a substrate
- Defining a metal system
- Integrating thin film resistors
- Designing with vias
- Incorporating high conductivity traces
- Use of multi-layer thin films
- Substrate singulation

RESOURCES

- For technical questions contact EFI@vishay.com
- For additional information, visit www.vishay.com/company/brands/electro-films

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THIN FILM SUBSTRATES

Design Guide

Advanced thin film manufacturing capabilities have been developed by Vishay EFI to address custom substrate needs by bridging the gap between ultra high levels of silicon and GaAs integration and traditional chip and wire “hybrid” design approaches. Using a wide array of ceramic substrate materials and metal systems, combined with advanced thin film manufacturing features and capabilities, the circuit designer can now easily reduce circuit size and parts count over traditional thin film substrate design approaches, while also enhancing performance. Vishay EFI offers a variety of thin film technologies to meet a wide range of industry requirements, all supported by a completely captive quick-turn prototype to high volume manufacturing facility.

Using This Guide

The Vishay EFI Thin Film Design Guide is a multi-sectioned document created to help our customers understand how to integrate thin film technologies in their designs. This guide provides a roadmap for the design process starting with substrate material selection and ending with finished product singulation. Adherence to the design rules and material selections presented here will lead to a highly reliable and high performing custom thin film solution.

Choosing a Substrate

Substrate selection will determine both electrical and mechanical performance. Vishay EFI has the capability to deposit thin film structures on a wide range of materials, allowing designers the freedom to select the substrate most suitable for the given application.

The electrical performance is influenced mainly by the dielectric constant of the material. The most commonly used substrate for high frequency applications is alumina. This material offers constant dielectric performance over a wide frequency range. Other materials that are used regularly include quartz and titanate ceramics. The former is used due to its low dielectric constant and thermo-mechanical stability. The later is desirable due to its high dielectric constant. Vishay EFI also has extensive experience processing magnetic materials such as ferrites for applications including circulators and isolators.

Mechanical specifications, including thermal conductivity (TC) and coefficient of thermal expansion (CTE), become critical parameters for high power designs where heat conduction and induced stresses are of concern. Materials including beryllia, aluminum nitride, and quartz are often chosen for their functional-specific mechanical properties. Common applications for these materials are detailed in Table 1.

Table 1: Common substrate materials and their applications

Material	Typical Uses	Comments
Alumina (Al_2O_3)	Low to medium power DC / microwave circuits using Si, GaAs, or GaN ICs; Edge-coupled filters and power dividers	Cost-effective material with wide range of applications
Aluminum Nitride (AlN)	High power DC / microwave circuits using Si, GaAs, or GaN ICs	Optimal CTE match with silicon devices
Beryllia (BeO)	High power DC / microwave circuits using Si, GaAs, or GaN ICs; High power terminations	Extremely high thermal conductivity
Quartz	Microwave / millimeter-wave circuits requiring extremely low loss or low CTE	Low loss tangent and CTE with very smooth optical surface finish
Titanate*	RF / microwave filter or oscillators requiring high Q resonators; capacitors	Dielectric constants available from 12 to 500
Ferrite*	RF / microwave circulators / isolators	Magnetically activated material
Sapphire*	Millimeter-wave / optical circuits with special electrical or mechanical requirements	Low loss tangent and optical surface finish

* Call factory for availability

Table 2 summarizes the key mechanical and electrical properties of various substrate materials and the available level of thin film capability integration as defined in this design guide. Additional capabilities, not described in Table 2, are available upon request.

Table 2: Common mechanical and electrical properties by material

Material	Dielectric Constant ε at 1 MHz*	Tan δ at 1 MHz / 10 GHz*	Dielectric Strength KV/mm (V/mil)*	Surface Finish (µin CLA)	Coefficient of Thermal Expansion (ppm/°C)*	Thermal Conductivity (W/m°C) at 25 °C / 100 °C*	Common Thickness (mils / mm)
Alumina (Al_2O_3)	9.9	0.0001	(380 at 0.025)	< 1 (pol) < 12 (lap) < 4 (a.f.)	7.0	26.6	5 to 40 (0.127 to 1)
Aluminum Nitride (AlN)	8.8	0.0005 0.002	(355)	< 4 (pol) 10 to 20 (lapped)	4.6	190 Min / 160 170 Min / 130	5 to 40 (0.127 to 1)
Beryllia (BeO)	6.7	-	20 (230)	< 3 (pol) 15 to 40 (lap)	9.0	320 / 270 285 / 240	10 to 90 (0.254 to 2.3)
Quartz	4.5	0.00002 0.0001	(> 635)	60 / 40	0.55	5 / 2	10 to 40 (0.254 to 1.0)
Titanate**	-	-	-	-	-	-	-
Ferrite**	-	-	-	-	-	-	-
Sapphire**	-	-	-	-	-	-	-

* Typical values
** Call factory

In general, thick substrate materials are recommended to simplify handling issues and minimize costs. However, other considerations can influence the desired substrate thickness. Vishay EFI regularly processes alumina, AlN, and quartz down to 5 mils thick.

Additionally, the surface finish of the ceramic material can play a role in the overall performance of the circuit. Ceramic surface quality is commonly described by three grades: as-fired, lapped, and polished. The surface quality of the ceramic substrate will influence parameters such as the resolution of the photo-patterning process or the loss of high frequency signals.

Defining a Metal System

Vishay EFI offers several different metals to meet the custom needs of our customer base. For simple conductor / resistor circuits, the designer enjoys the most flexibility in their choice of metal system due to the simpler process requirements of these types of circuits. As the complexity and level of integration increase, the list of available metal system choices narrows to allow for tighter process control and manufacturability. Each metal deposited on the surface of the substrate serves a specific purpose, namely that of resistor, adhesion, barrier, or conductor layer. Table 3 identifies the specific function of the available metals as well as their available thickness ranges.

Table 3: Available metals and their functions			
Layer Type	**Metal**	**Range of Values**	**Comments**
Resistor	Tantalum nitride (TaN)	20 Ω/sq to 125 Ω/sq	TCR to ± 50 ppm/°C
	Nickel chromium (NiCr)	25 Ω/sq to 225 Ω/sq	TCR to ± 25 ppm/°C
Adhesion	Titanium tungsten (TiW)	250 Å to 750 Å	Ideal for high temperatures
	Chromium (Cr)	250 Å to 750 Å	Ideal for low temperatures
Barrier	Nickel (Ni) to sputtered	750 Å to 2000 Å	Standard barrier
	Palladium (Pd)	750 Å to 2000 Å	High to temp solder barrier
Conductor	Gold (Au)	10 µin to 200 µin (0.25 µm – 5 µm)	
	Copper (Cu)	10 µin to 200 µin (0.25 µm – 5 µm)	
	Aluminum (Al)	60 µin to 120 µin (1.5 µm to 5 µm)	Aluminum wire bond
High Current Conductor	Gold (Au)	200 µin to 1000 µin (5 µm to 25 µm)	See Table 14 for minimum line widths and spaces
	Copper (Cu)	200 µin to 4000 µin (5 µm to 100 µm)	

A metal system should be selected based upon electrical performance demands as well the assembly process requirements. Assembly requirements might include pads suitable for eutectic (solder) bonding and / or wire bonding.

Soldering pads are generally recommended to include a barrier layer designed to control the solubility of the pad metallization with the solder being applied. A nickel barrier layer is typically deposited under gold soldering pads to ensure reliable device attachment due to gold's high solubility in solders.

All of the standard metal systems offered by Vishay EFI are readily bonded using gold wire. For optimal bond integrity, a minimum of 100 µin (2.5 µm) gold thickness is recommended, although reasonable bonding results can be achieved with gold as thin as 50 µin (1.2 µm).

Intermetallic formation and barrier metal migration are influenced by film exposure to high temperatures. For this reason, it is important to select a metal system that can withstand the temperature profile requirements of the application. Table 4 provides a matrix of standard metal systems and assembly options.

Table 4: Standard metal systems and assembly options					
Metal System	Max. Reflow Temp. (°C)	Wire-Bondable Gold	Solder Type		
			Lead (Pb)-Free	Lead (Pb)- Bearing	Gold Bearing
Cr / Cu / Ni / Au	350	Yes	Yes	Yes	-
NiCr / TiW / Au	400	Yes	-	-	-
NiCr / Ni / Au	350	Yes	Yes	Yes	-
NiCr / TiW / Au / Ni / Au	350	Yes	Yes	Yes	-
TiW / Au	450	Yes	-	-	-
TiW / Ni / Au	350	Yes	Yes	Yes	
TiW / Au / Ni / Au	350	Yes	Yes	Yes	-
TiW / Pd / Au	450	Yes	-	-	Yes
TiW / Au / Cu / Ni / Au	350	Yes	Yes	Yes	-
TaN / TiW / Au	450	Yes	-	-	-
TaN / TiW / Ni / Au	350	Yes	Yes	Yes	-
TaN / TiW / Au / Ni / Au	350	Yes	Yes	-	-
TaN / TiW / Pd / Au	450	Yes	-	-	Yes
TaN / TiW / Au / Cu / Ni / Au	350	Yes	Yes	Yes	-

Additional metal system capabilities are available with Vishay EFI. These options are subject to review by the Vishay EFI engineering and production teams. Consideration will be given to special requests, with a focus on manufacturability and reliability.

Integrating Thin Film Resistors

If it is necessary to embed resistive elements in the design to achieve high precision voltage division, current regulation, or matched power termination, Vishay EFI offers thin film resistors of lithographically patterned tantalum nitride (TaN) or nickel chromium (NiCr). The resistive film should be selected based upon application-specific requirements such as performance, assembly packaging needs, and temperature exposure. Table 5 summarizes the key standard parameters of these resistor materials.

Table 5: Standard thin film resistor parameters					
Material	TCR (ppm/°C)	Standard Sheet Resistivity 99.6 % Al_2O_3 (Ω/sq)	Standard Sheet Resistivity AlN, BeO (Ω/sq)	Stability*	Tolerance**
TaN	± 50	20 to 125	25 to 100	< 0.1 %	0.1 % to 20 %
NiCr	± 25	25 to 225	50 to 150	< 0.1 %	0.1 % to 20 %

* 1000 hours at 125 °C in air
** Special tolerances available

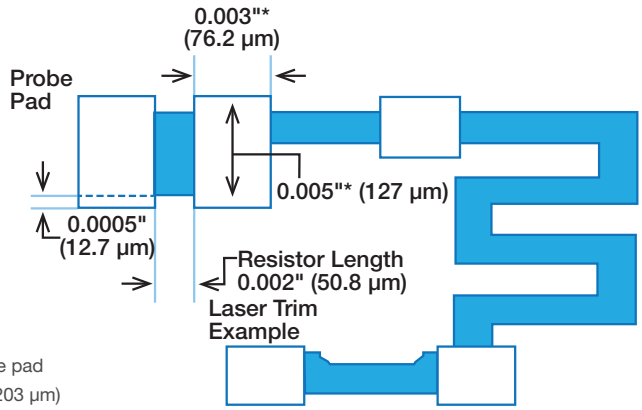
To ensure compliance with these parameters, the design engineer must consider the self-heating effects of the operating resistor and understand the power dissipation characteristics of the environment. A complete thermal analysis should be performed by the design engineer to ensure proper thin film resistor design. Table 6 lists current density standards for common materials.

Table 6: Current density

Sheet Resistance	Al_2O_3	Silicon	Quartz	AIN	BeO
25 Ω/sq	4 mA/mil	20 mA/mil	0.5 mA/mil	19 mA/mil	32 mA/mil
50 Ω/sq	2 mA/mil	10 mA/mil	0.25 mA/mil	9.5 mA/mil	16 mA/mil
100 Ω/sq	1 mA/mil	5 mA/mil	0.125 mA/mil	4.7 mA/mil	8 mA/mil
200 Ω/sq	0.5 mA/mil	2.5 mA/mil	0.062 mA/mil	2.3 mA/mil	4 mA/mil

After the thin film resistor values have been determined and a metallization film selected, the thin film resistor layout can be designed. There are two typical approaches for accomplishing this: the block-style resistor (see Figure 1) or serpentine-style resistor (see Figure 2). With both design approaches, it is standard to employ a laser trim process to trim the resistor to the desired value and tolerance. Vishay EFI employs both scrub (edge) trimming and plunge trimming techniques to achieve the desired resistor value.

Figure 1. Probe Pad Requirements (Minimum)



* For resistors < 1000 ohms, use probe pad size of 0.006 in (152 µm) x 0.008 in (203 µm)

Figure 2. Serpentine Resistor With Two Areas for Laser Trim

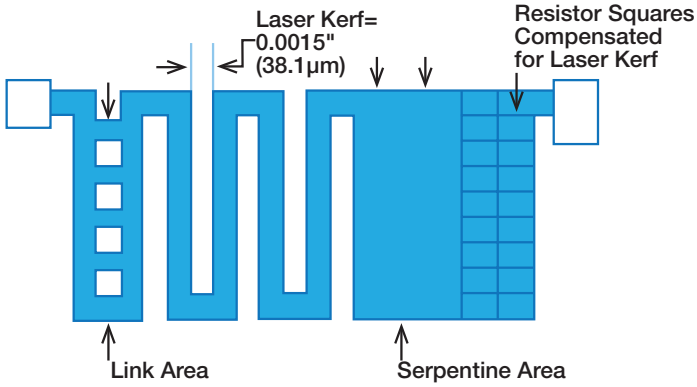


Table 7 indicates the basic design rule standards for integrated thin film resistors.

Table 7: Resistor design rules		
Parameter	**Value**	**Comment**
Min. resistor dimension	0.002 in x 0.002 in (50 µm x 50 µm)	
Min. probe pad dimension	0.003 in x 0.005 in (75 µm x 127 µm)	For resistors < 1000 Ω, use probe pad size of 0.006 in (152 µm) x 0.008 in (203 µm)
Resistor layout dimensions (block resistor / serpentine resistor)	100 % of nominal value / 100 % of nominal resistor value plus laser kerfs of 0.5 mil²/sq	
Resistor trim	Scrub, plunge, or bake to value	Bake to value ± 10 % or 20%

Designing With Vias

Electrical connections can be made from the front to the backside of the substrate through the use of metallized via holes. Vishay EFI offers two types of vias: plated-through vias and solid-metal filled vias.

Vishay EFI has more than 25 years of experience delivering thin film substrates with both plated and filled via configurations. Plated vias are used in low power applications and in instances where the designer has a requirement to leave the via open through the center. The typical design rule is that the via diameter is not less than 80 % of the nominal substrate thickness. Table 8 summarizes design rules for plated-through vias.

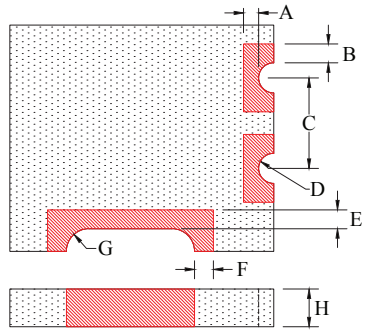
Table 8: Plated-through via design rules				
Substrate Thickness (in (mm))	**Plated Via Diameter (in (mm))**	**Minimum Capture Pad Diameter (in (mm))**	**Minimum Via Spacing Center to Center**	**Minimum Via Spacing Center to Edge**
0.010 (0.250)	0.008 to 0.020 (0.175 to 0.508)	Diameter + 0.010 (Diameter + 0.250)	2x diameter	1.5x diameter
0.015 (0.375)	0.012 to 0.030 (0.300 to 0.762)	Diameter + 0.010 (Diameter + 0.250)	2x diameter	1.5x diameter
0.020 (0.500)	0.016 to 0.040 (0.400 to 1.016)	Diameter + 0.010 (Diameter + 0.250)	2x diameter	1.5x diameter
0.025 (0.625)	0.020 to 0.050 (0.500 to 1.27)	Diameter + 0.010 (Diameter + 0.250)	2x diameter	1.5x diameter

*Plated-through vias available on all substrate materials

Plated-through vias can also be used on the perimeter of a substrate where edge castellations are required. This design approach allows for traditional surface-mount solder techniques to be used at the next assembly.

Figure 3 shows a typical substrate with edge castellations. All of the design rules as indicated in Table 8 apply to edge castellations as well.

Figure 3.



Dimension	Description
A	0.005 in minimum capture pad B side: same minimum size capture pad
B	≥ 0.005 in
C	≥ 3x hole diameter
D	Diameter ≥ 0.8 Substrate thickness (H) 0.010 in minimum
E	0.005 in minimum capture pad
F	0.005 in minimum capture pad
G	0.006 in ± 0.002 in minimum
H	Substrate thickness 0.010 in minimum

Solid-metal filled vias provide the circuit designer with a solid-metal filled via structure that offers the lowest possible thermal resistance, lowest possible RF inductance, and highest packaging density of any of the via technologies. Table 9 details performance characteristics of solid-metal filled vias and Table 10 summarizes their design rules.

Table 9: Solid-metal filled via performance characteristics

Filled Via Metal	Thermal Conductivity (W/mK)	Filled Via Resistance / Inductance							
		Via Height / Via Diameter							
		0.010 in / 0.007 in		0.015 in / 0.008 in		0.020 in / 0.010 in		0.025 in / 0.13 in	
Gold (Au)	300	230 µΩ	0.06 nH	260 µΩ	0.10 nH	220 µΩ	0.14 nH	160 µΩ	0.17 nH

Table 10: Solid-metal filled via design rules

Substrate Thickness (in (mm))	Filled Via Diameter (in (mm))	Minimum Capture Pad Diameter (in (mm))	Minimum Via Spacing Center to Center	Minimum Via Spacing Center to Edge
0.010 (0.250)	0.008 to 0.015 (0.200 to 0.380)	Diameter + 0.005 (Diameter + 0.125)	2x diameter	1.5x diameter
0.015 (0.375)	0.008 to 0.022 (0.200 to 0.560)	Diameter + 0.005 (Diameter + 0.125)	2x diameter	1.5x diameter
0.020 (0.500)	0.010 to 0.030 (0.250 to 0.760)	Diameter + 0.005 (Diameter + 0.125)	2x diameter	1.5x diameter
0.025 (0.625)	0.013 to 0.037 (0.330 to 0.940)	Diameter + 0.005 (Diameter + 0.125)	2x diameter	1.5x diameter

*Solid-metal filled vias are available in Al2O3, AlN, and BeO substrates

There are also a variety of other mechanical features that must be considered when designing with both plated-through and solid filled vias. These features are summarized in Table 11.

Table 11: Via mechanical features		
Parameter	**Value**	**Comment**
Filled via surface planarity	+0.0002 in / -0.0006 in (+5 µm / - 15 µm)	
Via location tolerance	±0.002 in (± 50 µm)	From a fixed datum
Via diameter tolerance	±0.002 in (± 50 µm)	Measured from drill entry surface

Incorporating High Conductivity Traces

Vishay EFI's capability to deposit very thick conductor traces has enabled design approaches that allow high current, low resistance circuit traces to co-exist with microwave structures and transmission lines. For circuit traces carrying high currents over long distances, the resistive losses of thin film conductor lines can become significant. By selectively increasing the thickness of high current lines, the engineer can now have fine line RF structures on the same circuit with low loss DC lines. Additionally, these low resistance traces can be used to manage thermal loads within RF circuits.

Typically, the design engineer will calculate the trace resistance (R_{total}) of a structure during the design process. The trace resistance is defined as:

R_{total} = (trace length / trace width) x conductor sheet resistance
R_{total} = (L/W) x R_{sheet}

The sheet resistance (R_{sheet}) is derived by dividing the bulk resistivity by the conductor thickness. Therefore, the thicker one can deposit the conductor, the lower the overall sheet resistance. Table 12 details the bulk resistivity of common thin film metals, while Table 13 demonstrates the sheet resistance of typical thin film metals at a variety of deposition thicknesses.

Table 12: Selected bulk resistivity		
Material	**Theoretical Bulk Resistivity (µΩ *cm)**	**Conservative Value of Bulk Resistivity When Deposited (µΩ *cm)**
Gold (Au)	2.2	2.4 (sputtered) / 2.9 (plated)
Titanium tungsten (TiW)	-	45 (sputtered)
Copper (Cu)	1.71	2 (sputtered) / 4 (plated)
Nickel (Ni)	7	8.2 (sputtered)
Aluminum (Al)	2.7	3 (sputtered)

Table 13: Selected approximate sheet resistivities		
Metal	**Thickness (µ in (µm))**	**Plated Sheet Resistivity (mΩ/sq)**
Gold (Au)	80 (2)	14.5
Gold (Au)	160 (4)	7.25
Gold (Au)	400 (10)	2.9
Copper (Cu)	1000 (25)	0.42
Copper (Cu)	2000 (50)	0.21
Nickel (Ni)	200 (5)	160 (sputtered)
Aluminum (Al)	40 (1)	30 (sputtered)

In summary, gold (Au) and copper (Cu) can be deposited at much greater thicknesses than standard thin films to reduce overall conductor resistance. Au can be deposited up to a maximum thickness of 400 µin, while copper (Cu) can be plated routinely at thicknesses up to 4000 µin (100 µm). It is important to note that minimum line widths and spaces increase with film thickness. See Table 14 for a summary of line widths and spaces as associated with conductor thickness.

Table 14: High conductivity line widths and spaces

Plated Metals								
Metal thickness (µin / µm)	100 / 2.54	150 / 3.80	200 / 5.1	400 / 10.2	800 / 20.3	1000 / 25.4	2000 / 51	4000 / 102
Metal thickness tolerance (µin)	± 30	± 40	± 50	± 100	± 150	± 250	± 500	± 1000
Min. line width / space in (µm)	0.001 / 0.001 (25 / 25)	0.0015 / 0.0015 (38 / 38)	0.001 / 0.001 (25 / 25)			0.002 / 0.002 (50 / 50)	0.003 / 0.006 (75 / 150)	0.005 / 0.008 (125 / 200)
Line width / space tolerance in (µm)	± 0.0001 (2.5)	± 0.00015 (3.8)	± 0.0002 (5.0)	± 0.00025 (6.3)	± 0.0003 (7.5)	± 0.001 (25)	± 0.002 (50)	± 0.003 (76)
Sputtered Metals								
Metal thickness (µin / µm)	100 / 2.54	150 / 3.80	200 / 5.1	300 / 7.6				
Metal thickness tolerance (µin)	± 6	± 8	± 12	± 15				
Min. line width / space in (µm)	0.001 / 0.001 (25 / 25)	0.0015 / 0.0015 (38 / 38)	0.002 / 0.002 (50 / 50)	0.002 / 0.002 (50 / 50)				
Line width / space tolerance in (µm)	± 0.0001 (2.5)	± 0.0002 (5.0)	± 0.0003 (7.5)	± 0.0005 (12.5)				

Use of Multi-Layer Thin Film

Vishay EFI has developed a multi-layer thin film capability that allows for top-side insulated crossovers. Typical applications for this technology include Lange couplers (see Figure 4) and integrating a center-tapped thin film spiral inductor (see Figure 5), where polyimide supported air bridges are used to allow electrical connectivity to the isolated terminations.

Figure 4.

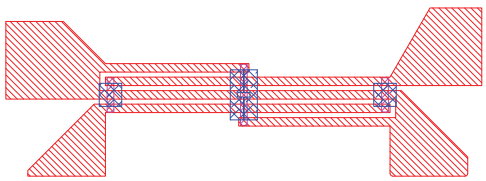
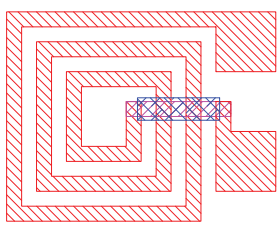


Figure 5.

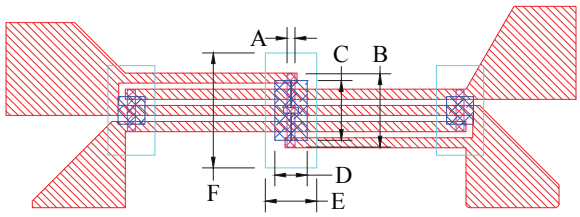


The integration of multi-layer crossovers is a well-established, robust process. However, strict adherence to material selection and design rule compliance is required to ensure proper functionality and reliability. Basic parameters and design rules are shown in Table 15.

Table 15: Multi-level crossover design parameters

Parameter		Minimum Value (in (µm))	Comments
Dimension	Crossover thickness	0.0001 (2.5)	Minimum
A	Crossover width	0.001 (25)	0.0001 in crossover to conductor pullback
B	Crossover length	0.003 (75)	Minimum
C / D	Insulator dimension	Length: 0.0015 (37.5) Width: 0.003 (76)	0.0025 in (63 µm) insulator-to-conductor overlap
	Insulator material		Polyimide
E / F	Encapsulation dimension	Crossover width: + 0.0015 (37.5) Crossover length: + 0.003 (76)	These values are added to the insulator dimension
	Encapsulation material		Polyimide

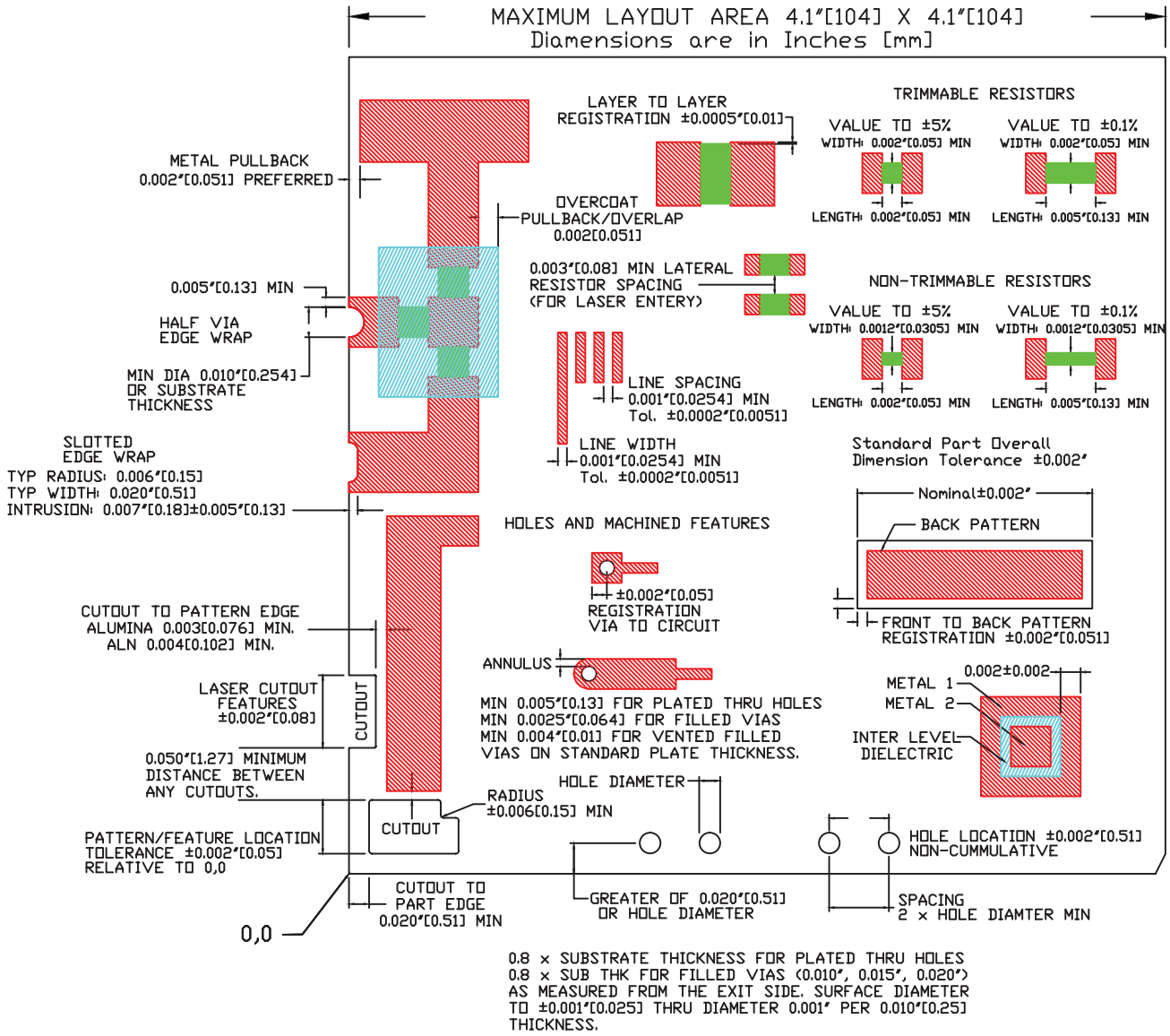
Figure 6. Lange Coupler



Substrate Singulation

Vishay EFI uses either traditional semiconductor dicing or CO_2 laser cutting for substrate singulation. These are both well-established processes and yield excellent results through manufacturing. Key dimension controls are defined in Figure 7 (following page). One technical requirement is that when CO_2 laser operations are required for either internal circuit cutouts, or external circuit profiles, the “B” side metallization must be pulled back from the cutting line by 0.003 in nominal. This is to ensure that the CO_2 laser does not come into contact with, and burn, the “B” side metals.

Figure 7.



THIN FILM SUBSTRATES
Design Guide

SEMICONDUCTORS

MOSFETs Segment

MOSFETs
- Low Voltage TrenchFET® Power MOSFETs
- Medium Voltage Power MOSFETs
- High Voltage Planar MOSFETs
- High Voltage Superjunction MOSFETs
- Automotive Grade MOSFETs

ICs
- VRPower® DrMOS Integrated Power Stages
- Power Management and Power Control ICs
- Smart Load Switches
- Analog Switches and Multiplexers

Diodes Segment

Rectifiers
- Schottky Rectifiers
- Ultrafast Recovery Rectifiers
- Standard and Fast Recovery Rectifiers
- High Power Rectifiers / Diodes
- Bridge Rectifiers

Small-Signal Diodes
- Schottky and Switching Diodes
- Zener Diodes
- RF PIN Diodes

Protection Diodes
- TVS TRANSZORB® and PAR® Diodes (unidirectional, bidirectional)
- ESD Protection Diodes (including arrays)

Thyristors / SCRs
- Phase Control Thyristors
- Fast Thyristors

Power Modules
- Input Modules (diodes and thyristors)
- Output and Switching Modules (contain MOSFETs, IGBTs, and diodes)
- Custom Modules

Optoelectronic Components Segment

Infrared Emitters and Detectors

Optical Sensors
- Proximity
- Ambient Light
- Light Index (RGBW, UV, IR)
- Humidity
- Quadrant Sensors
- Transmissive
- Reflective

Infrared Remote Control Receivers

Optocouplers
- Phototransistor, Photodarlington
- Linear
- Phototriac
- High Speed
- IGBT and MOSFET Drivers

Solid-State Relays

LEDs and 7-Segment Displays

Infrared Data Transceiver Modules

Custom Products

PASSIVE COMPONENTS

Resistors and Inductors Segment

Film Resistors
- Metal Film Resistors
- Thin Film Resistors
- Thick Film Resistors
- Power Thick Film Resistors
- Metal Oxide Film Resistors
- Carbon Film Resistors

Wirewound Resistors
- Vitreous, Cemented, and Housed Resistors
- Braking and Neutral Grounding Resistors
- Custom Load Banks

Power Metal Strip® Resistors

Battery Management Shunts

Crowbar and Steel Blade Resistors

Thermo Fuses

Chip Fuses

Pyrotechnic Initiators / Igniters

Variable Resistors
- Cement Variable Resistors
- Wirewound Variable Resistors
- Conductive Plastic Variable Resistors
- Contactless Potentiometers
- Hall Effect Position Sensors
- Precision Management Encoders

Networks / Arrays

RF and Microwave Resistors

High Voltage Resistors

Dividers

Non-Linear Resistors and Temperature Sensors
- NTC Thermistors
- PTC Thermistors
- Thin Film RTDs
- Varistors
- Platinum Chip Temperature Sensors

Magnetics
- Power Inductors
- Power Chokes
- High Frequency RF Inductors
- Magnetic Actuators
- Wireless Charging Coils
- Planar Devices
- Transformers
- Custom Magnetics

Connectors

Capacitors Segment

Tantalum Capacitors
- Molded Chip Tantalum Capacitors
- Molded Chip Polymer Tantalum Capacitors
- Tantalum MAP Capacitors
- Polymer Tantalum MAP Capacitors
- Coated Chip Tantalum Capacitors
- Solid Through-Hole Tantalum Capacitors
- Wet Tantalum Capacitors

Ceramic Capacitors
- Multilayer Chip Capacitors
- Disc Capacitors
- Multilayer Chip RF Capacitors
- Chip Antennas
- Thin Film Capacitors

Film Capacitors

Power Capacitors

Heavy-Current Capacitors

Aluminum Electrolytic Capacitors

ENYCAP™ Energy Storage Capacitors